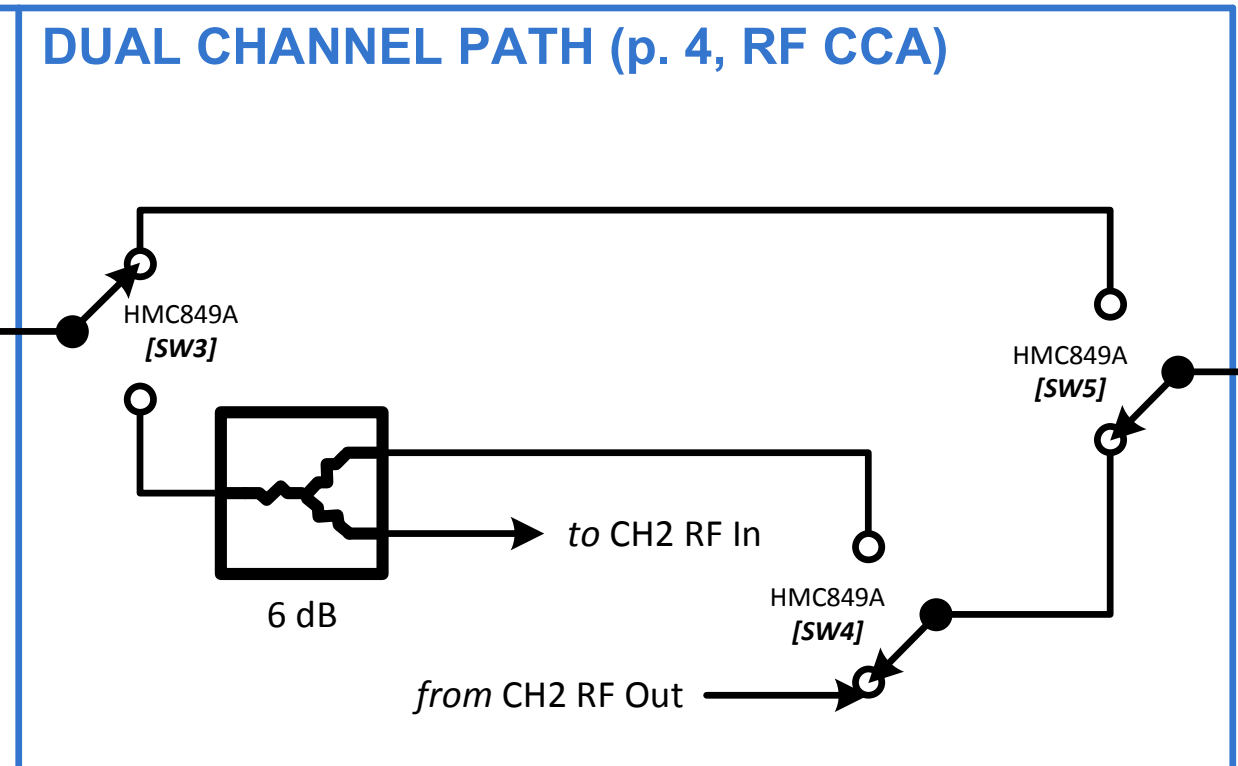
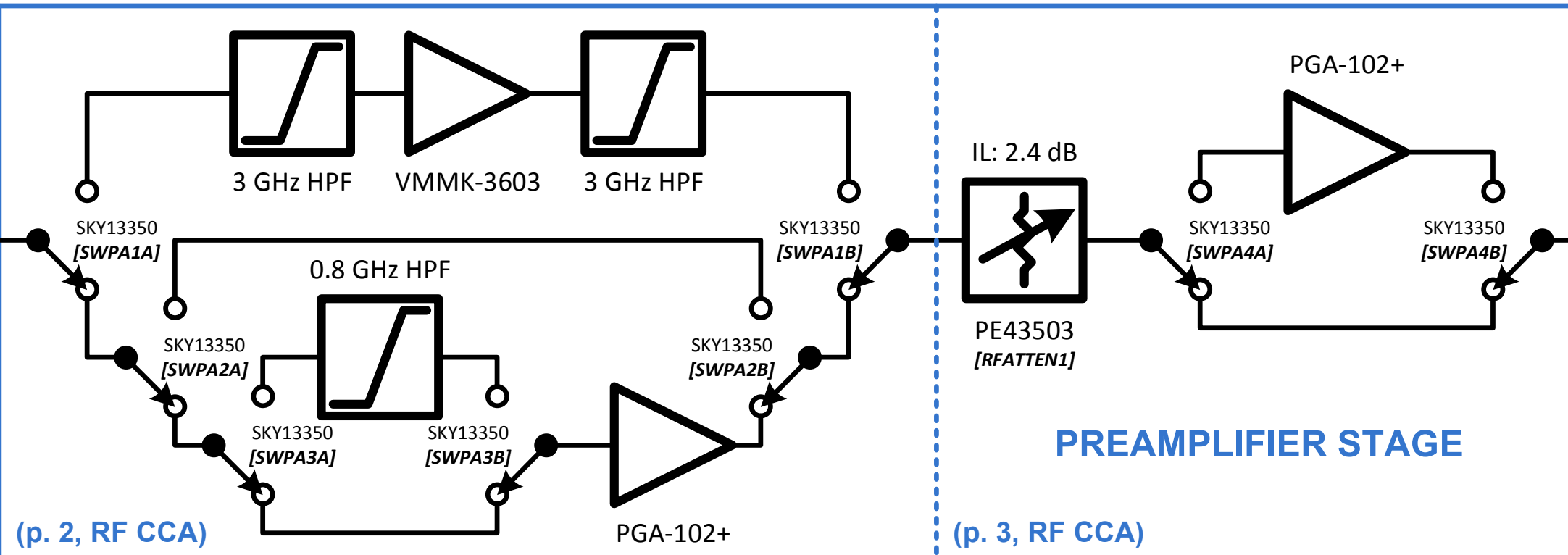
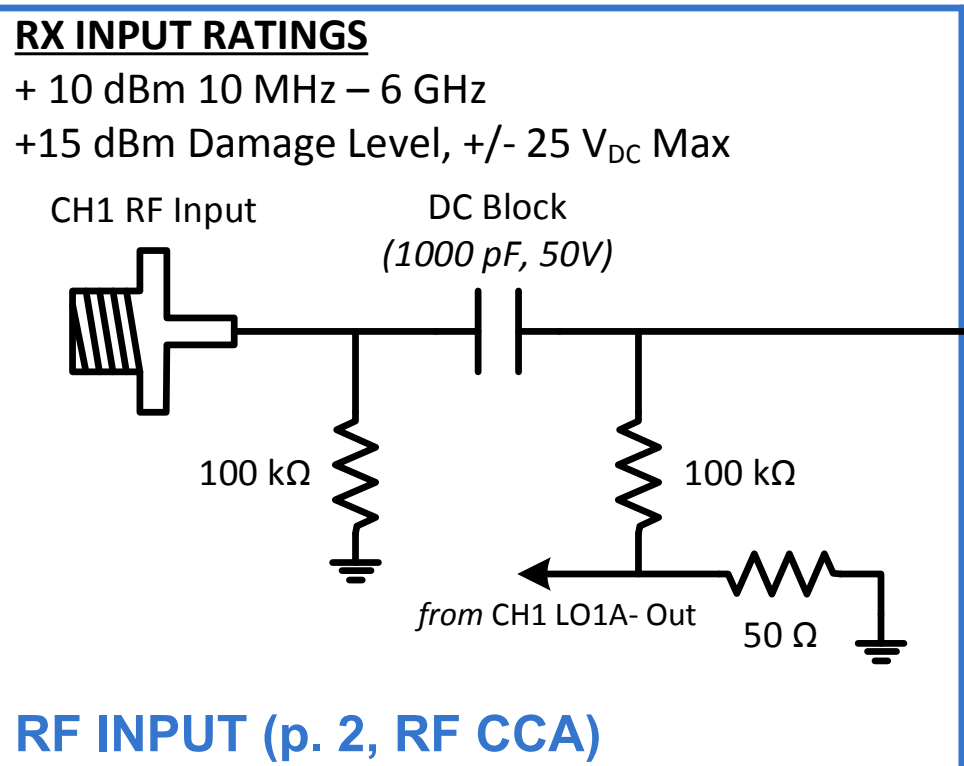
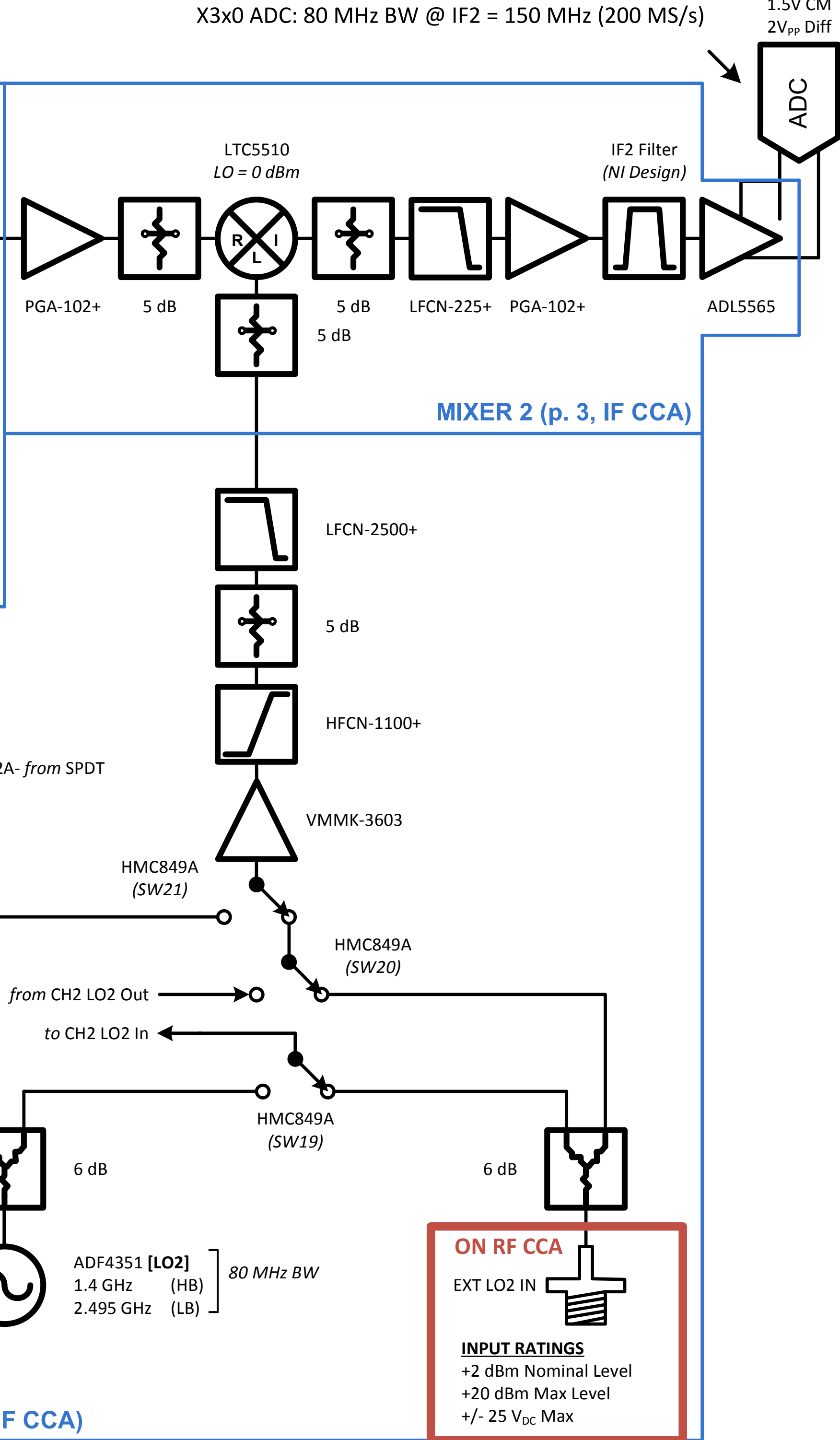
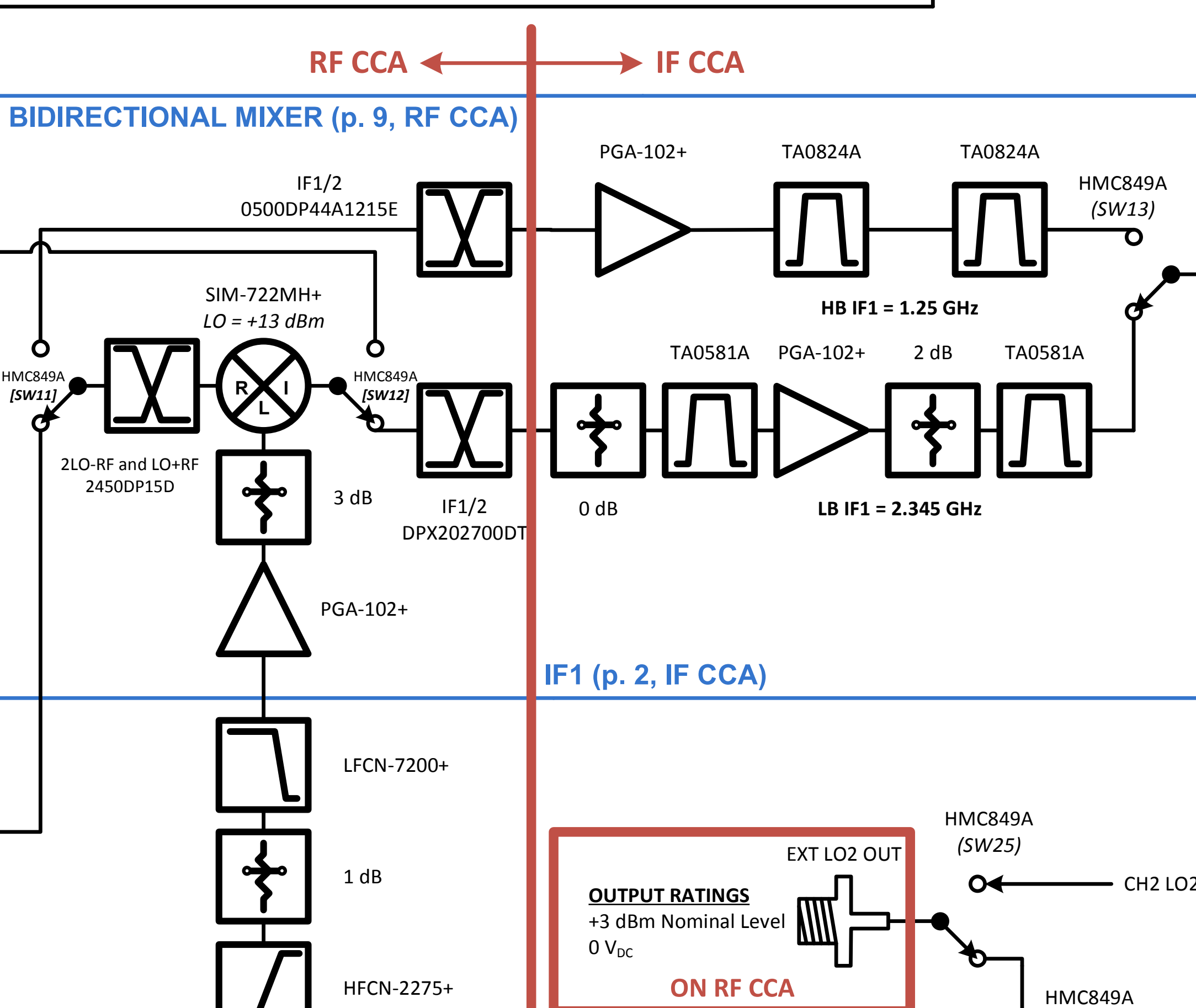
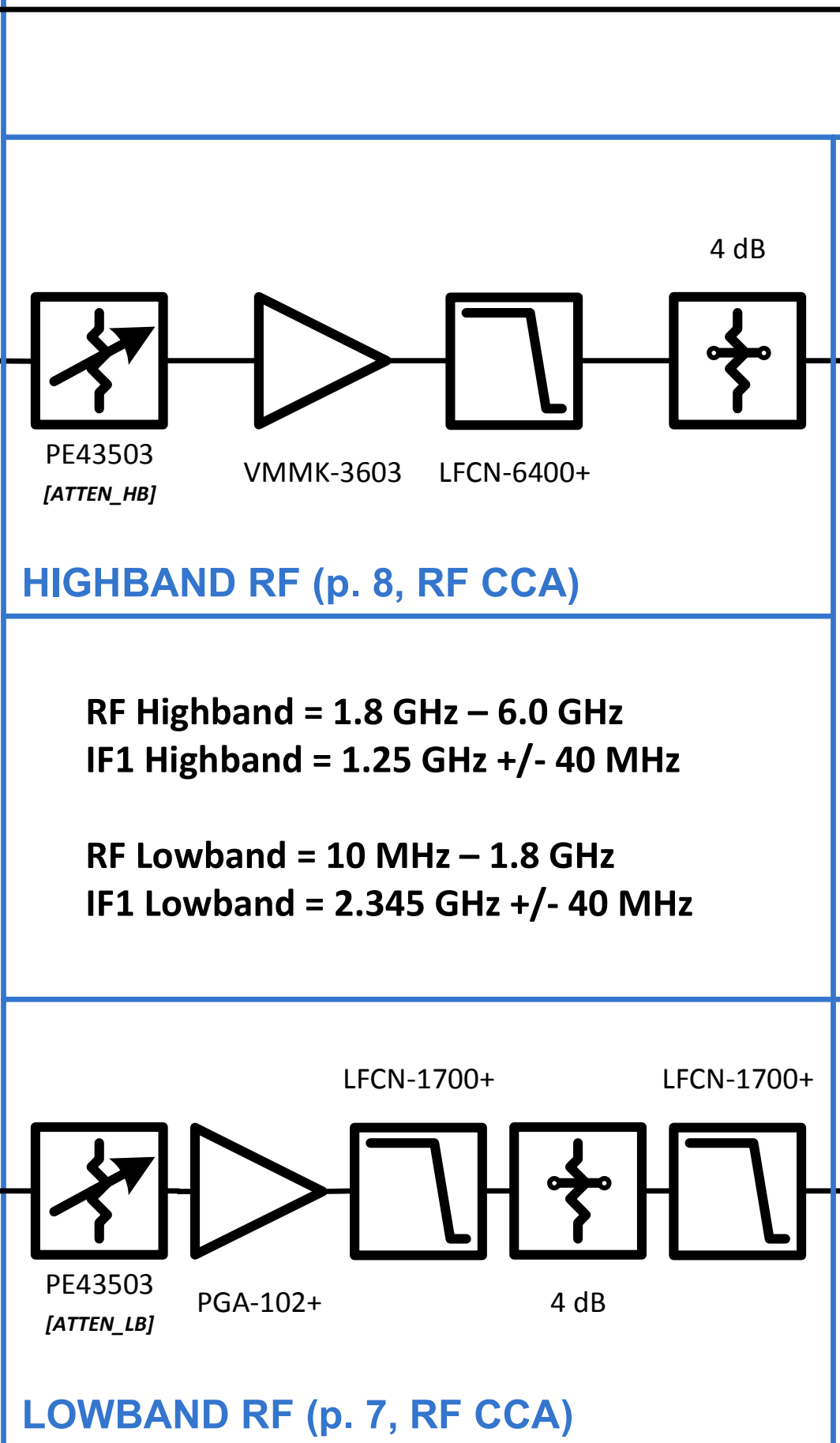
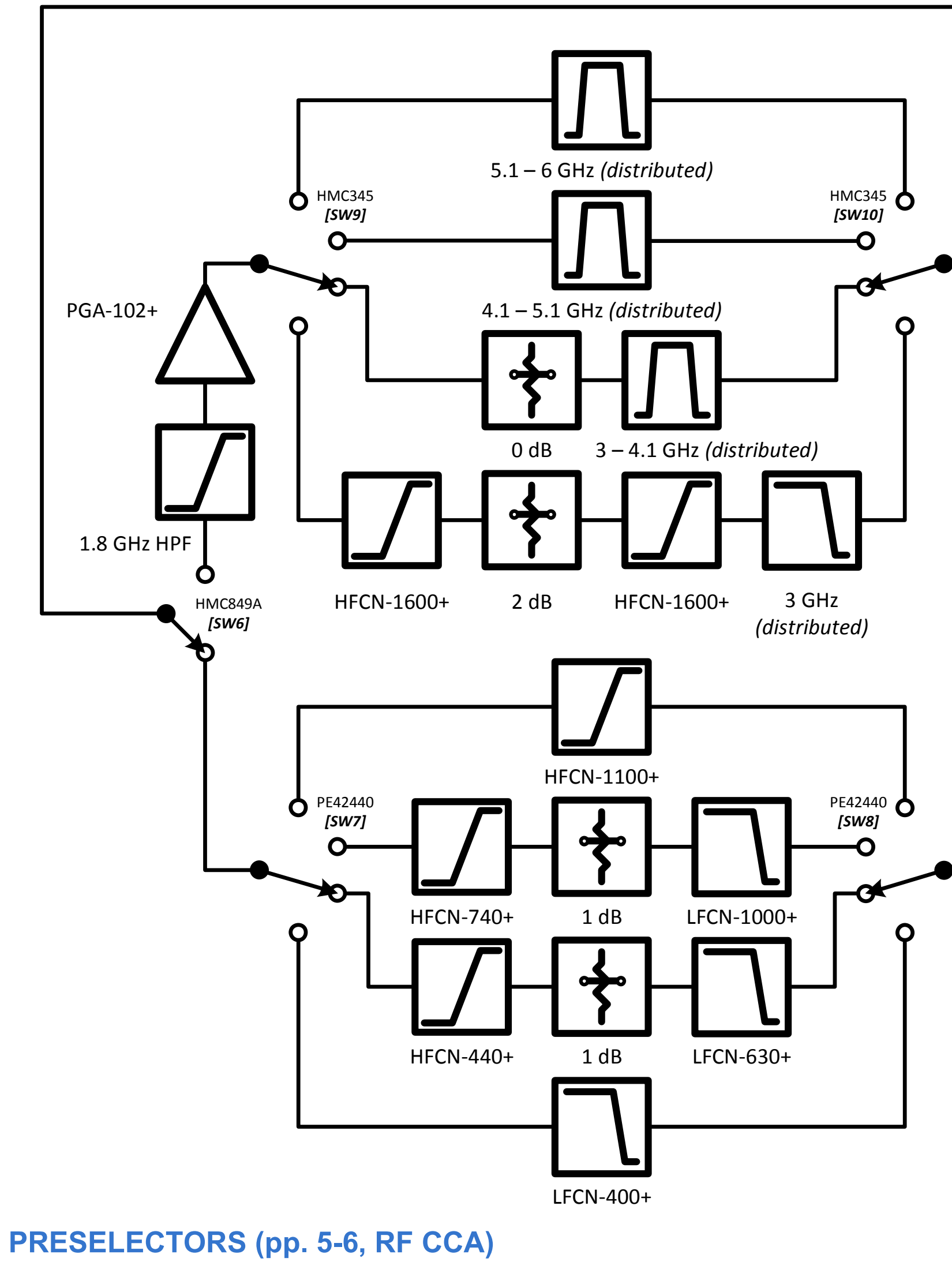


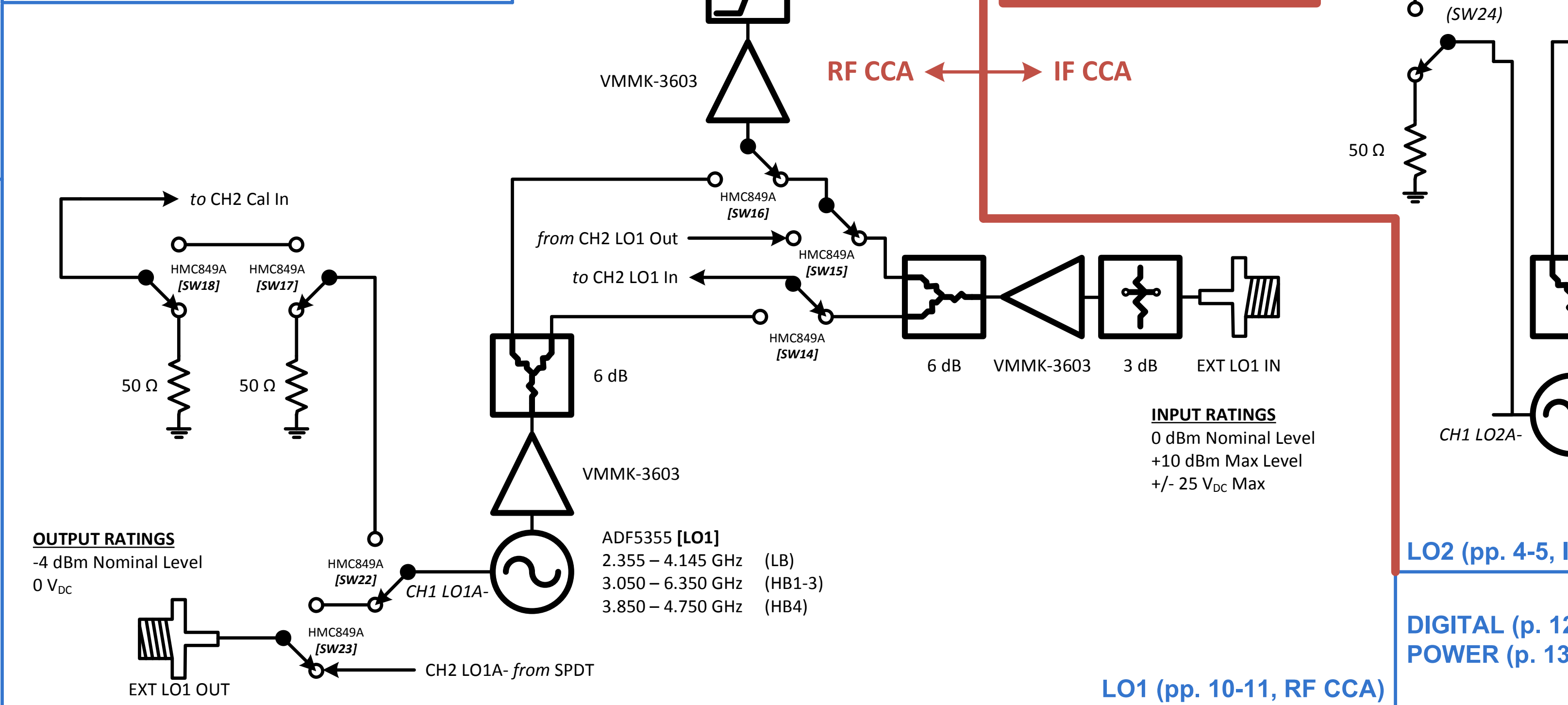


This block diagram represents one channel of a two-channel 10 MHz to 6 GHz superheterodyne daughterboard for the X3x0 (80 MHz BW) platform.

There are two LOs per channel, utilizing the ADF5355 and ADF4351 synthesizers, synchronized via FPGA I/O lines. Switchable LO input/output ports exist between channels.



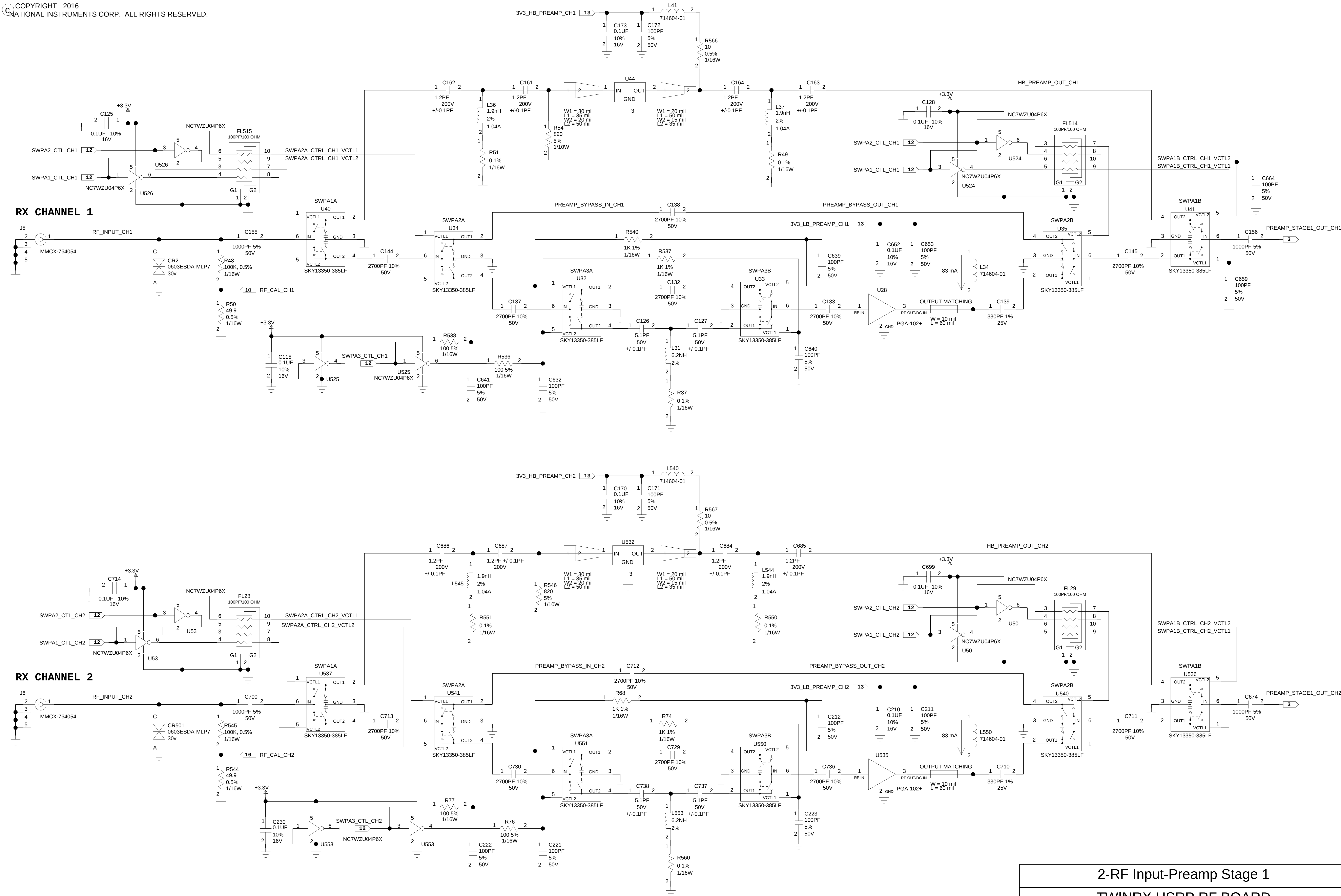
- Lowband Filters**
LB1: 10 – 500 MHz
LB2: 500 – 800 MHz
LB3: 800 – 1.2 GHz
LB4: 1.2 – 1.8 GHz
- Highband Filters**
HB1: 1.8 – 3.0 GHz
HB2: 3.0 – 4.1 GHz
HB3: 4.1 – 5.1 GHz
HB4: 5.1 – 6.0 GHz
- *each filter has a +/- 40 MHz band overlap*



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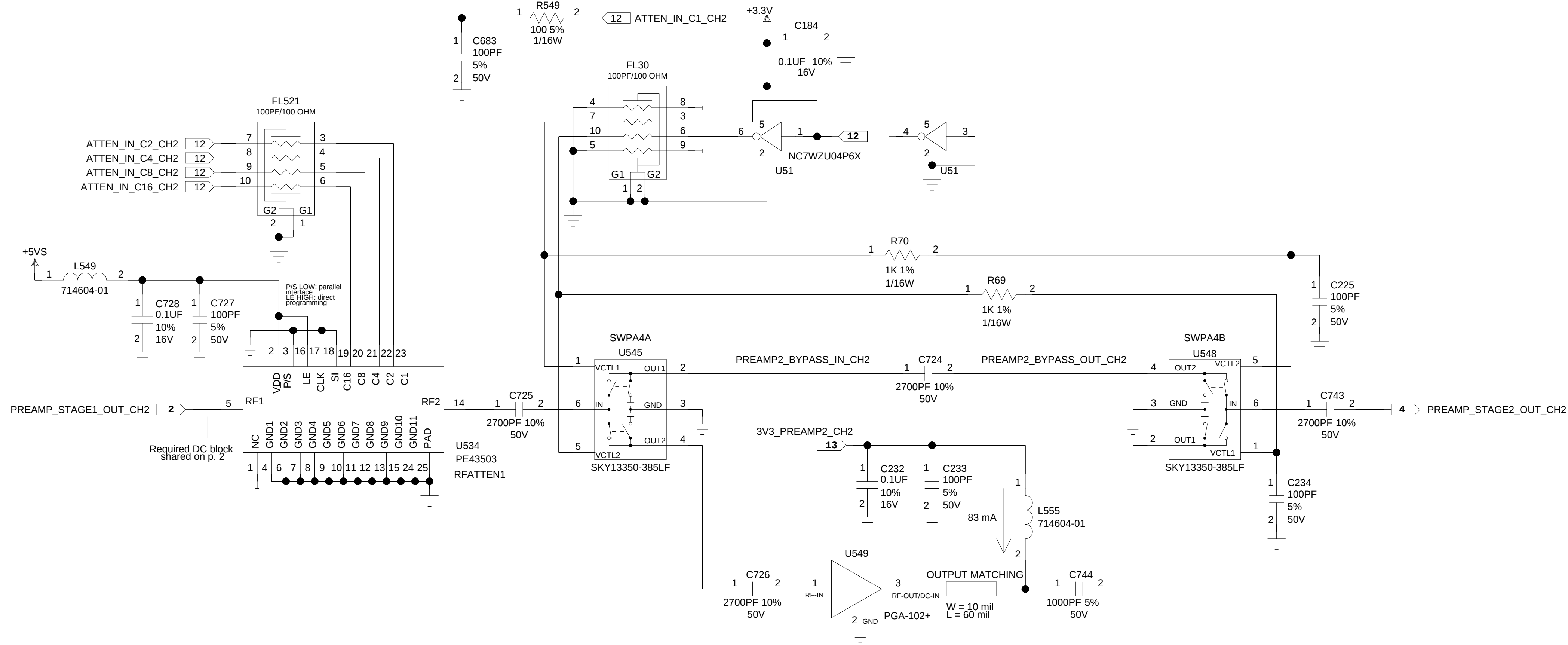
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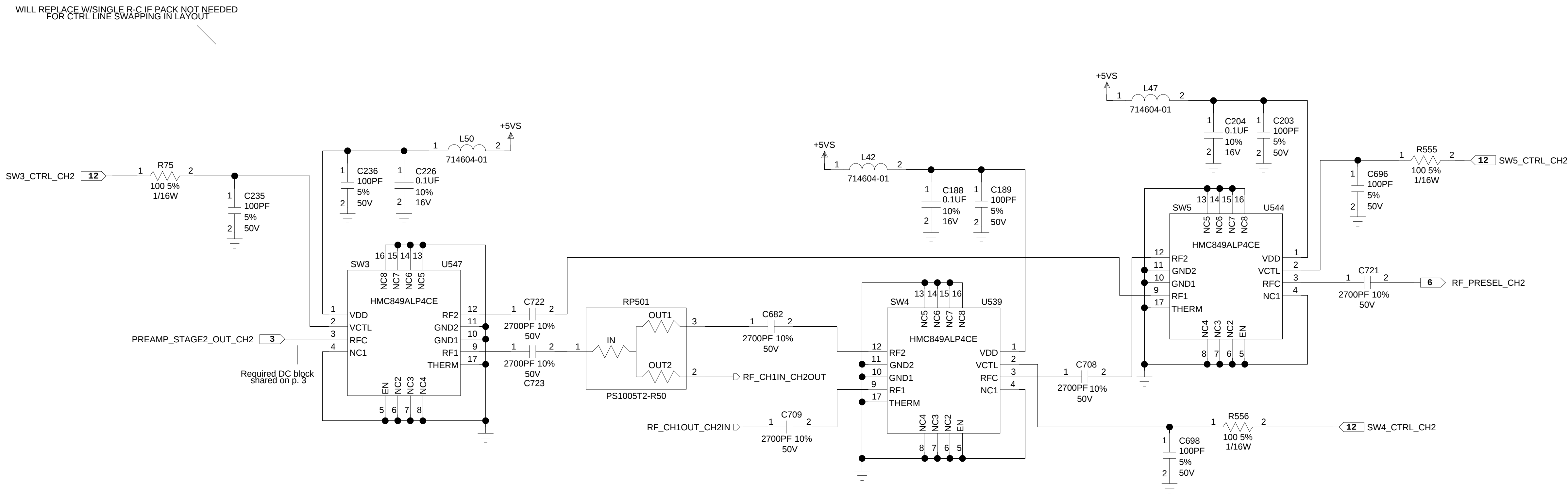
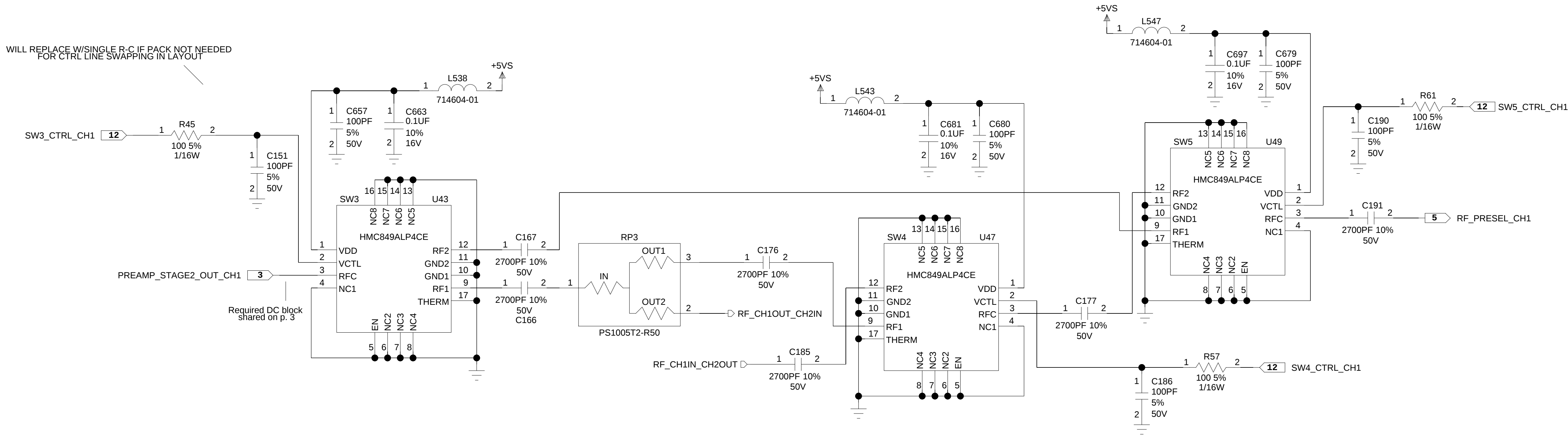


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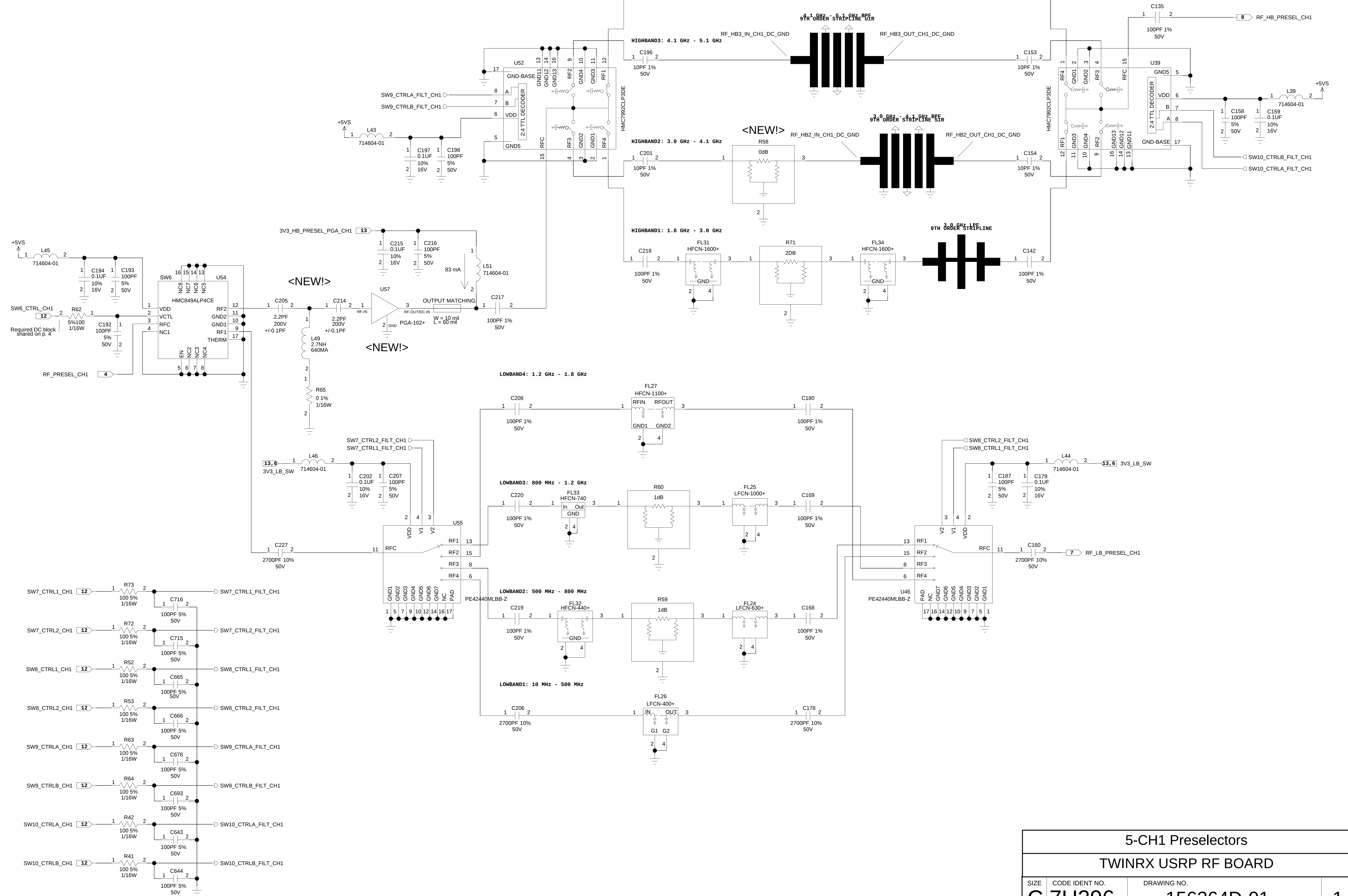
C

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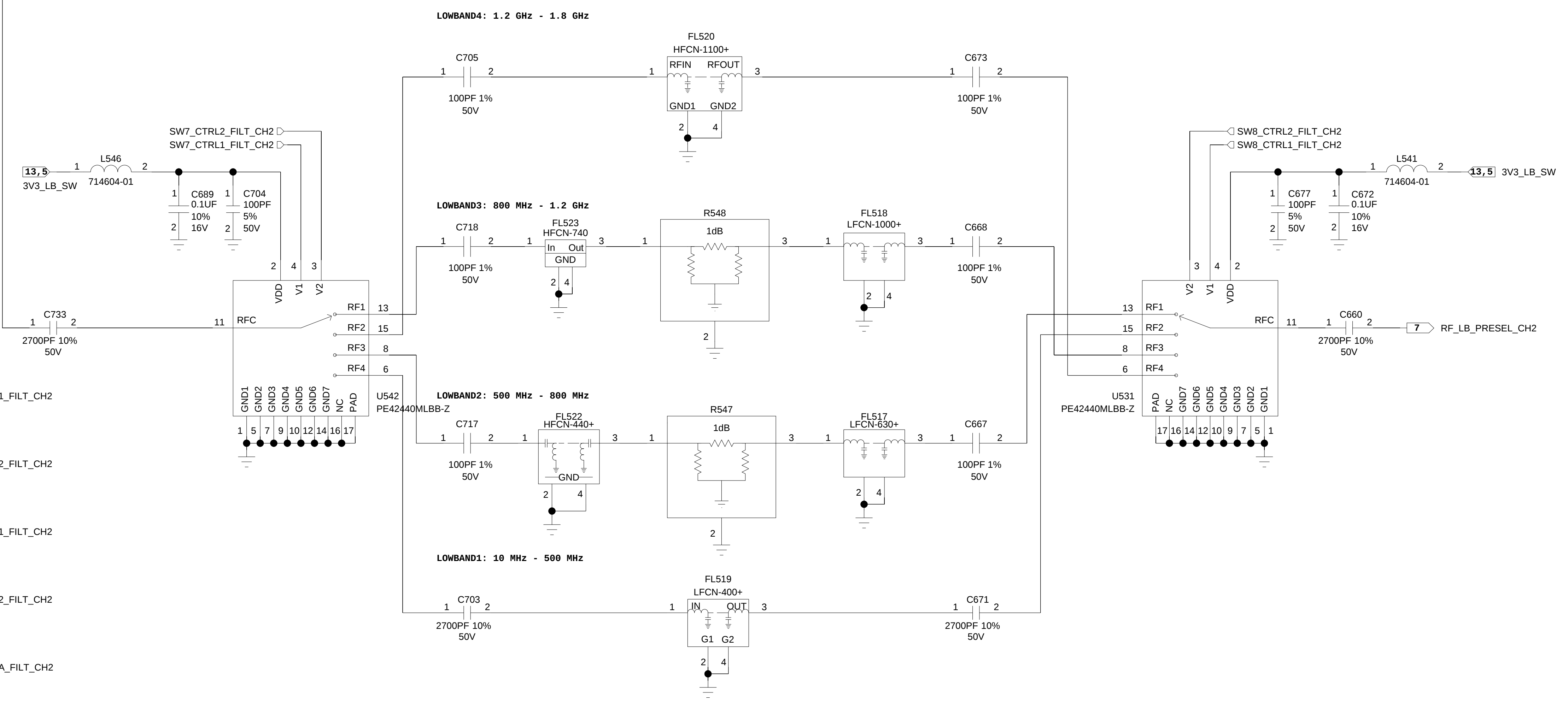
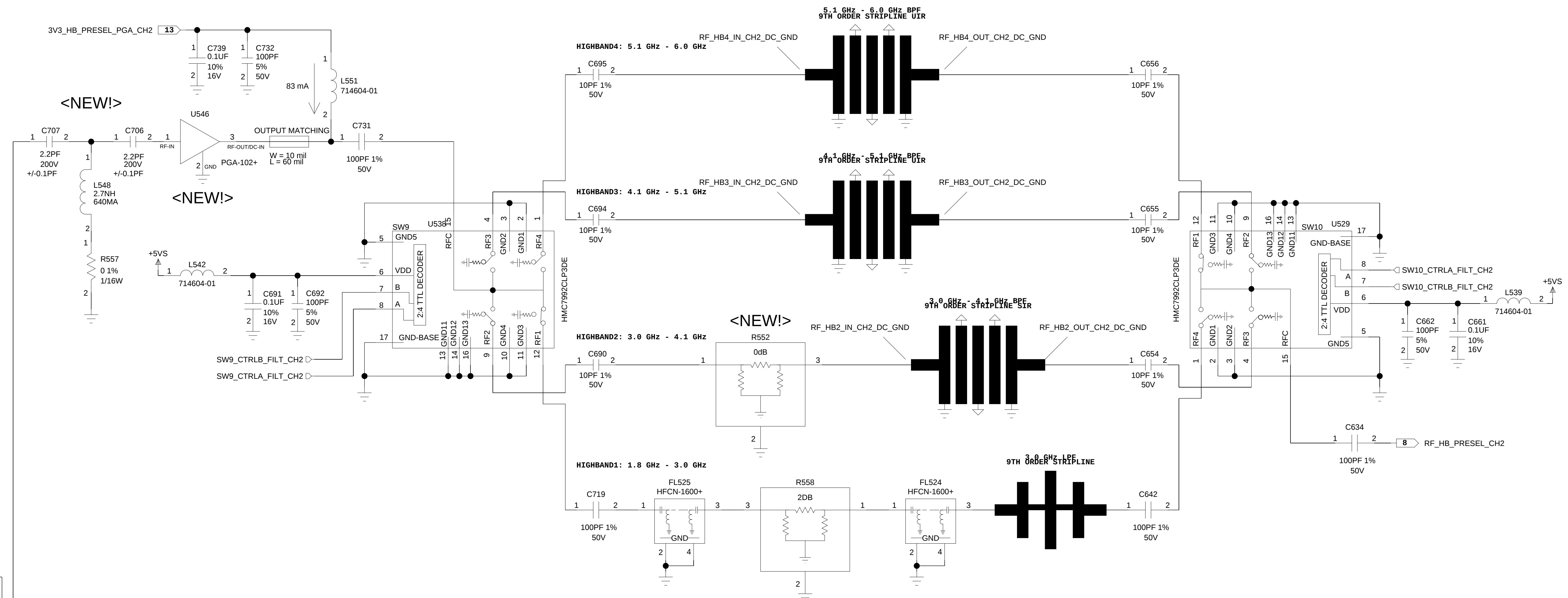
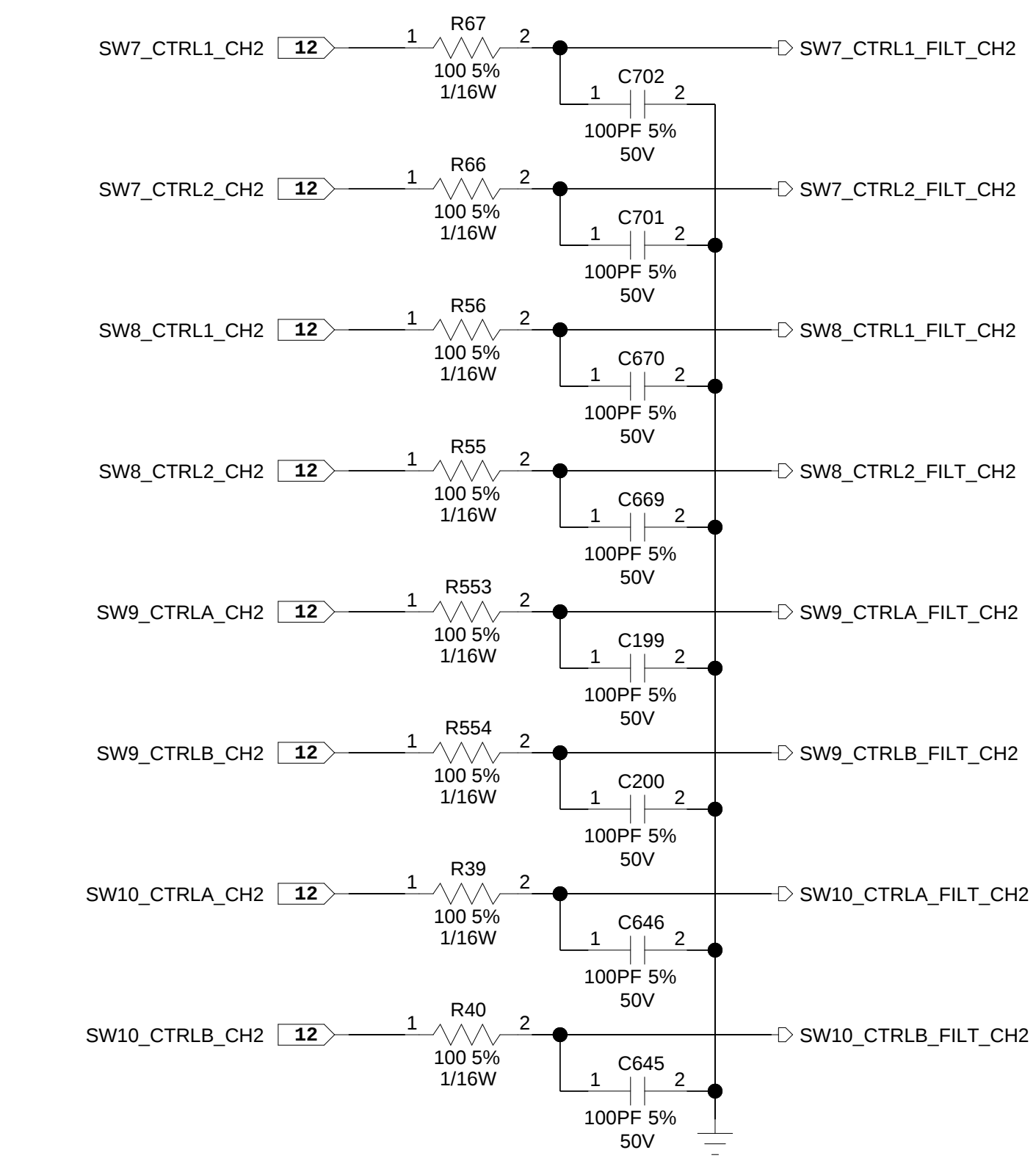
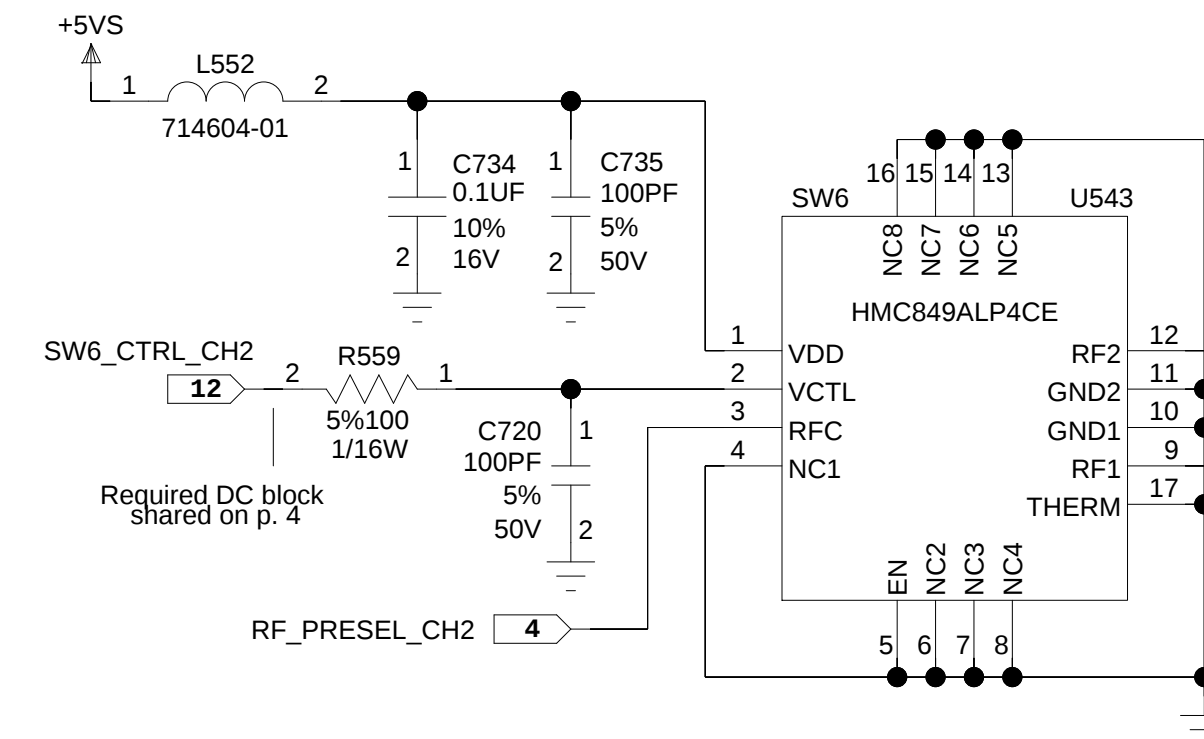
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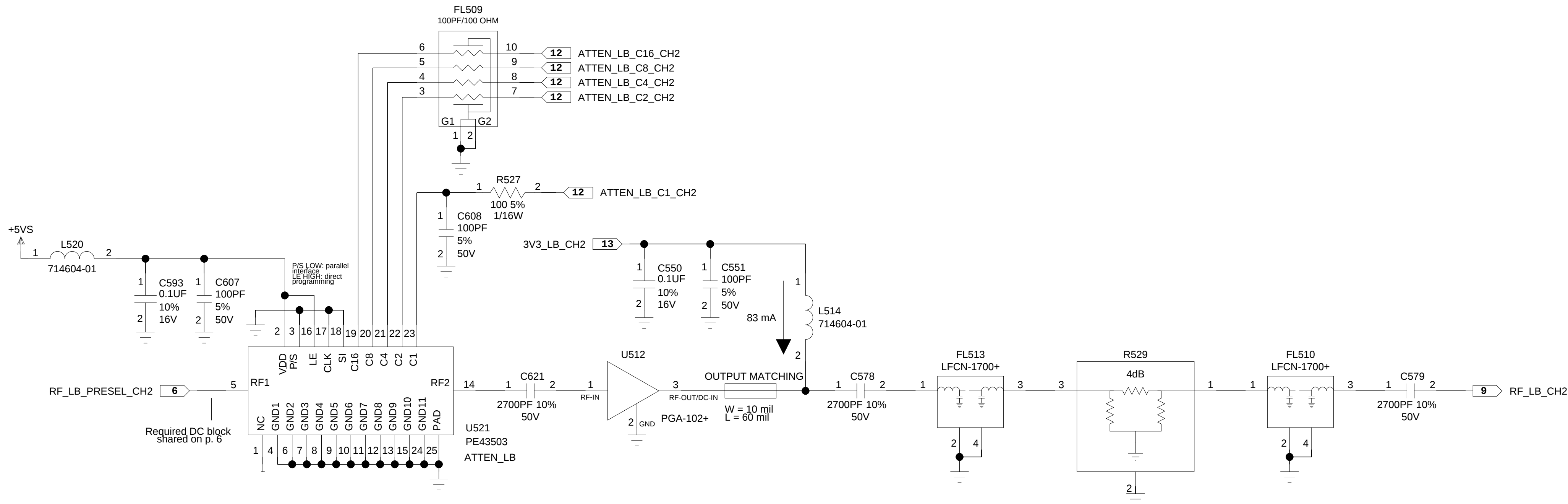
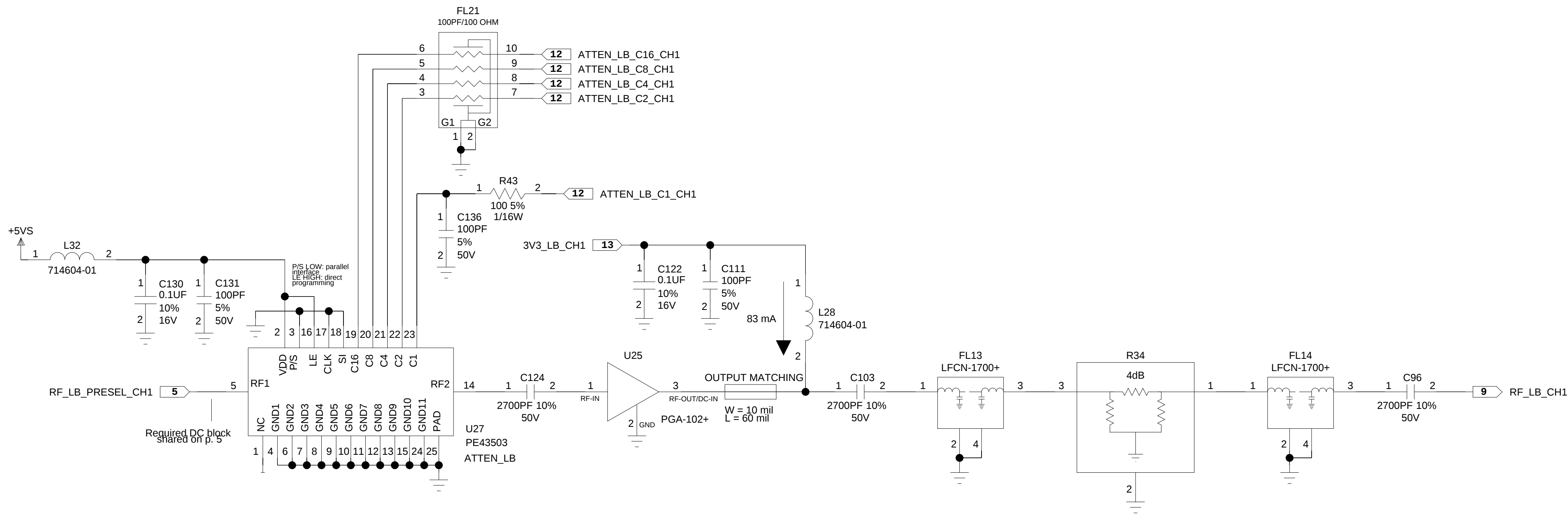
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6-CH2 Preselectors			
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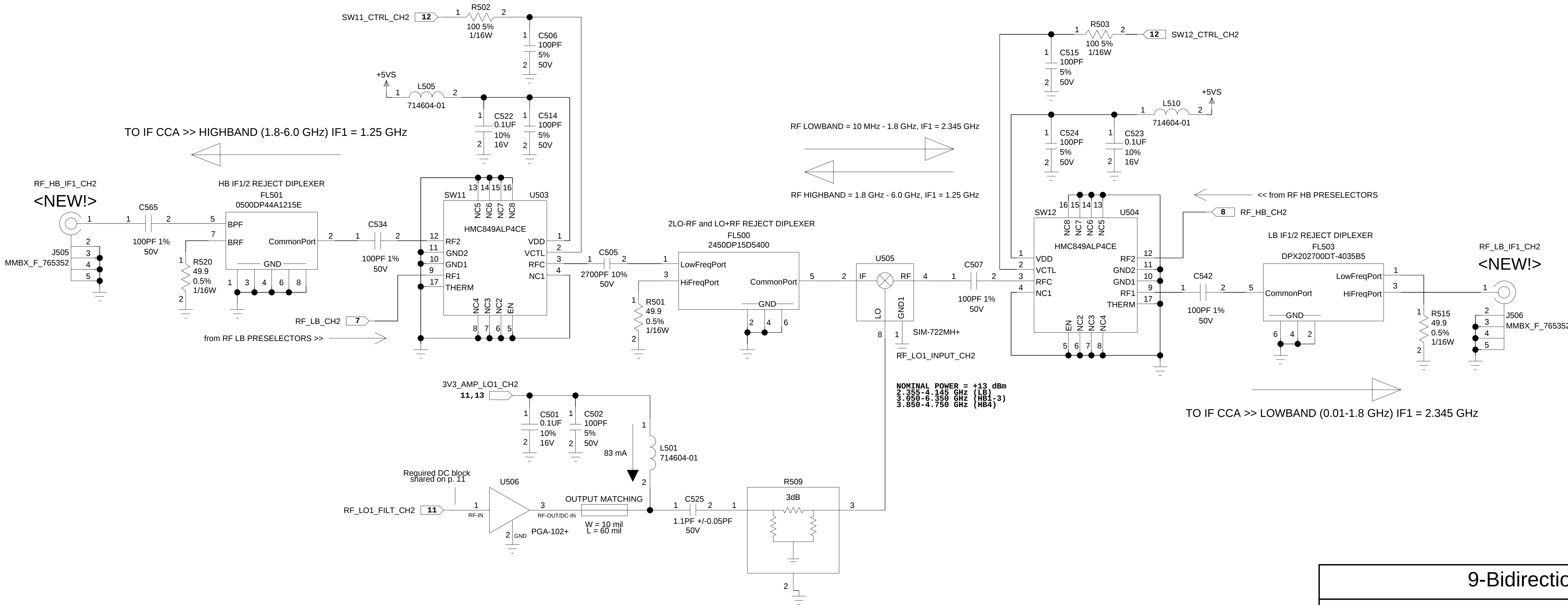
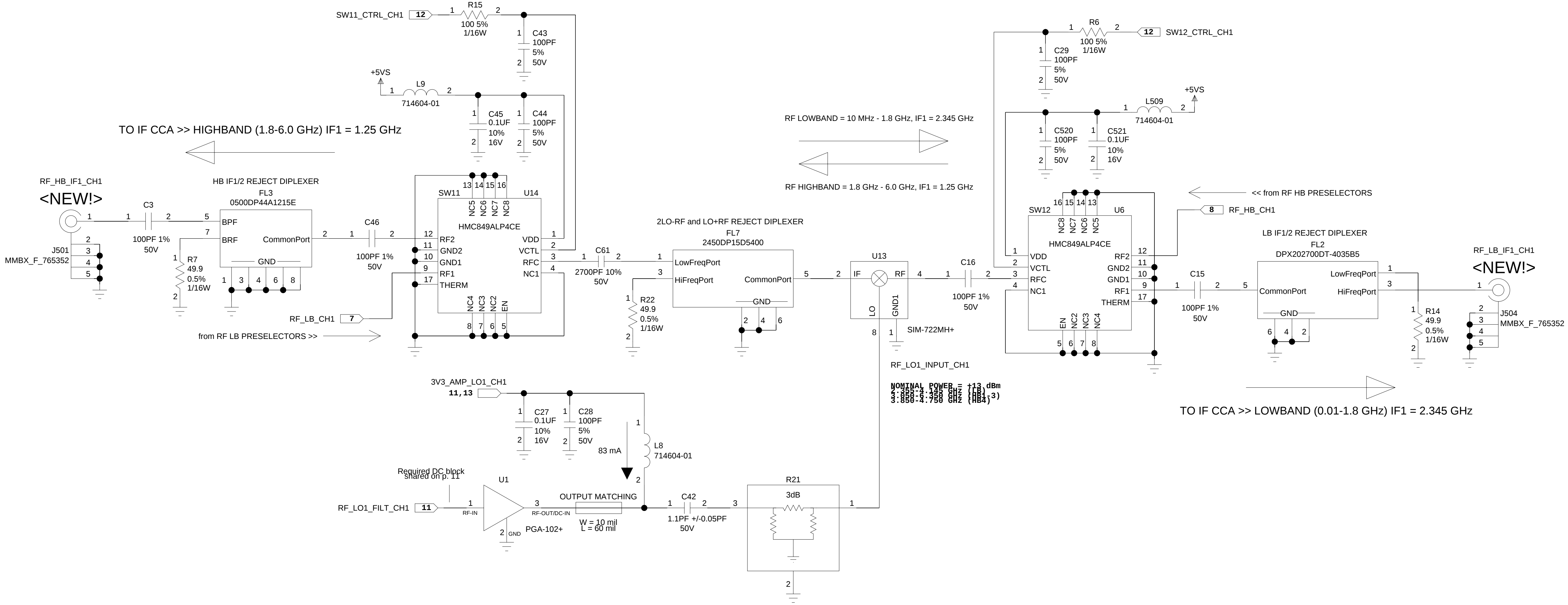
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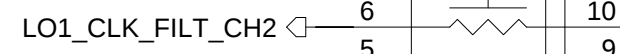
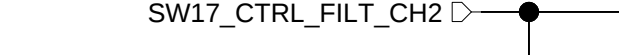
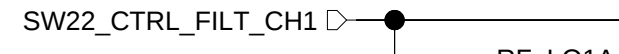
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9-Bidirectional Mixer			
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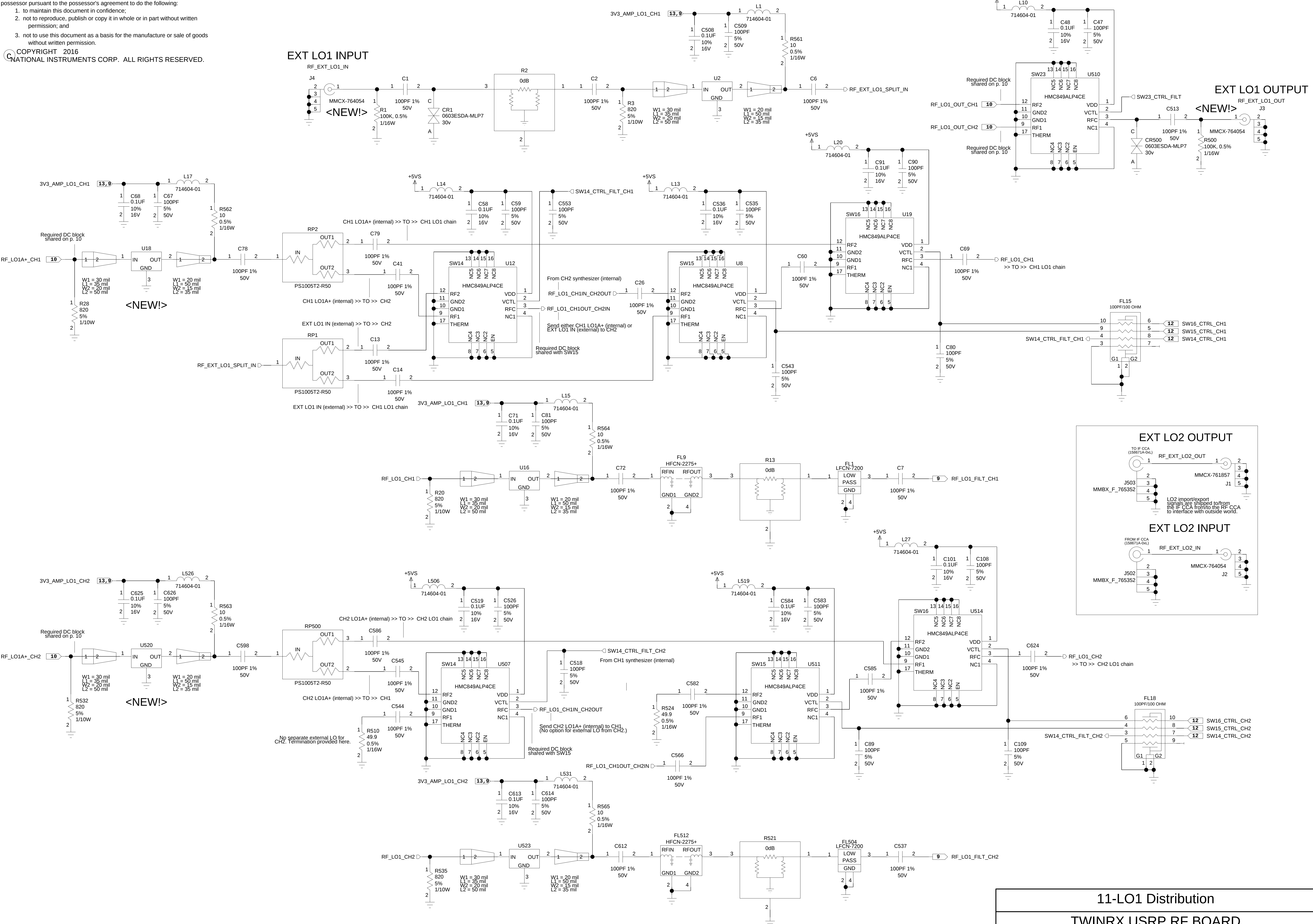
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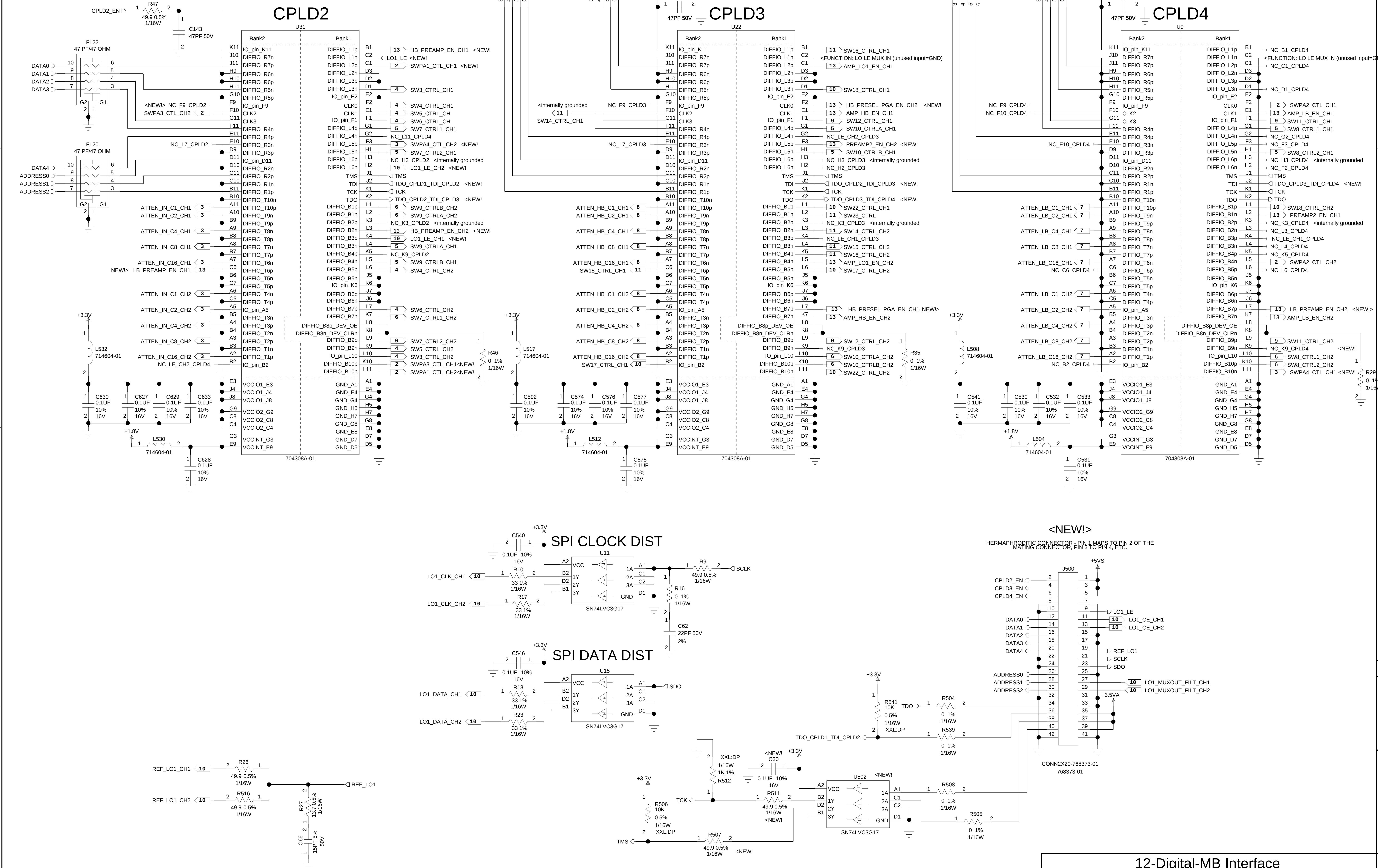
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11-LO1 Distribution			
TWINRX USRP RF BOARD			
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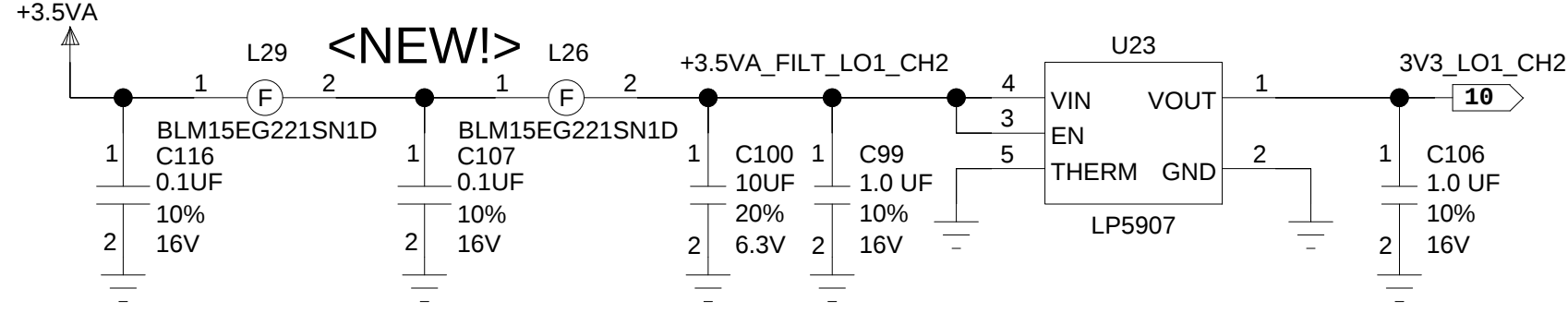
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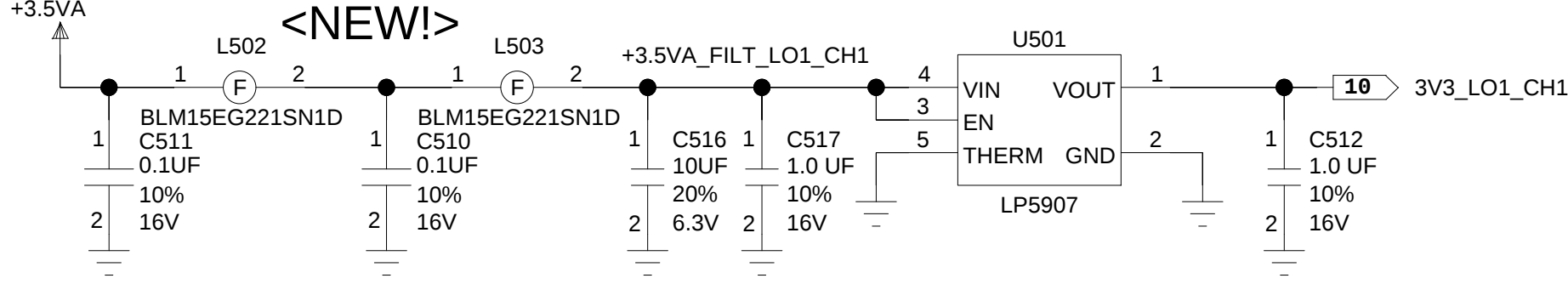
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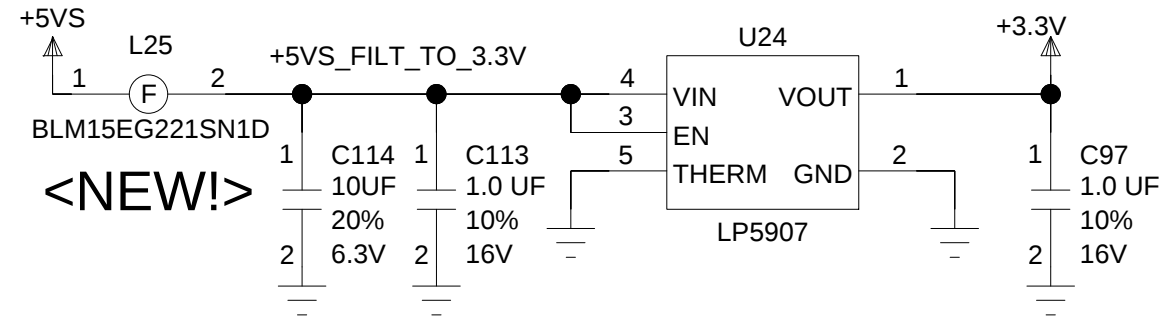
CH2 LO1 LDO: 3.72V to 3.3V



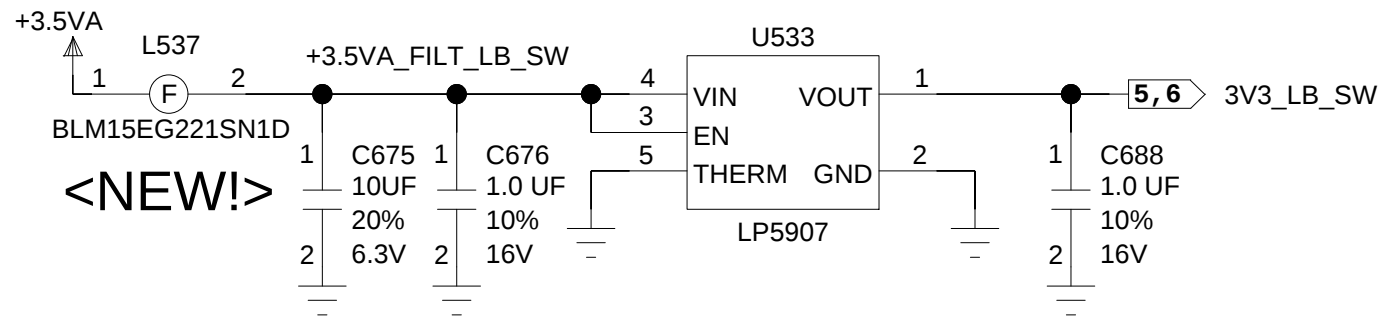
CH1 LO1 LDO: 3.72V to 3.3V



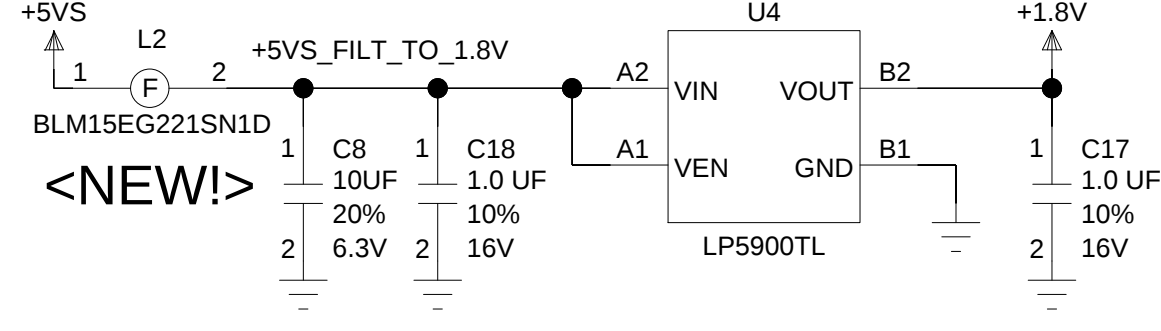
DIGITAL LDO: 5V to 3.3V



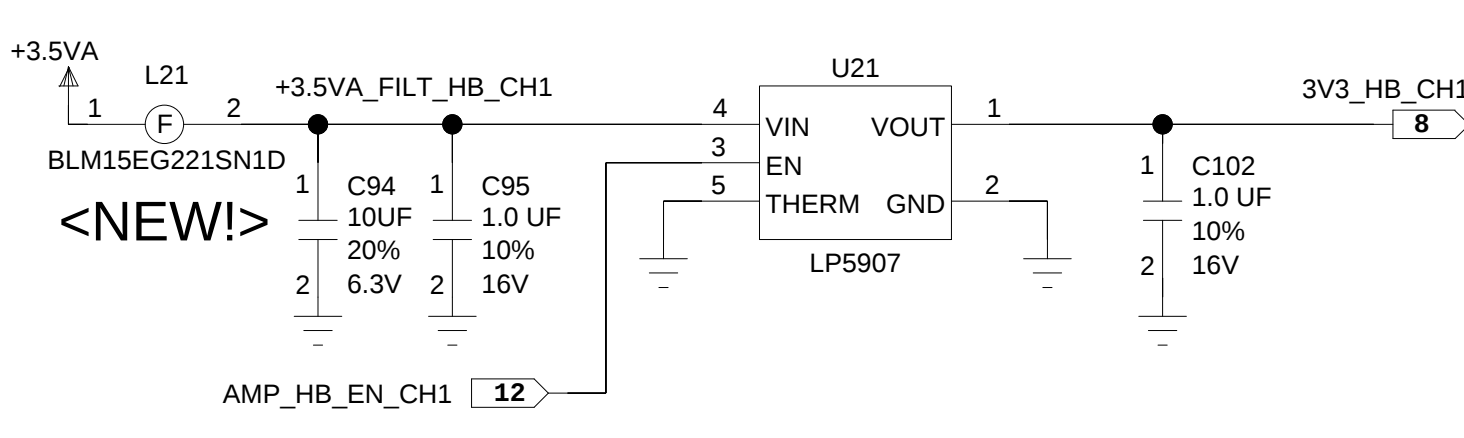
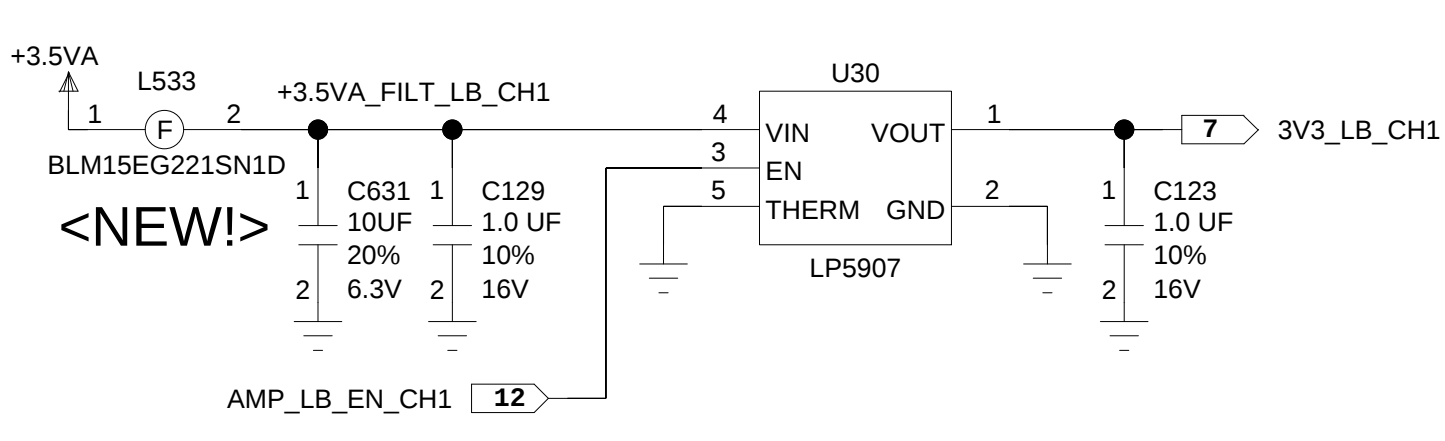
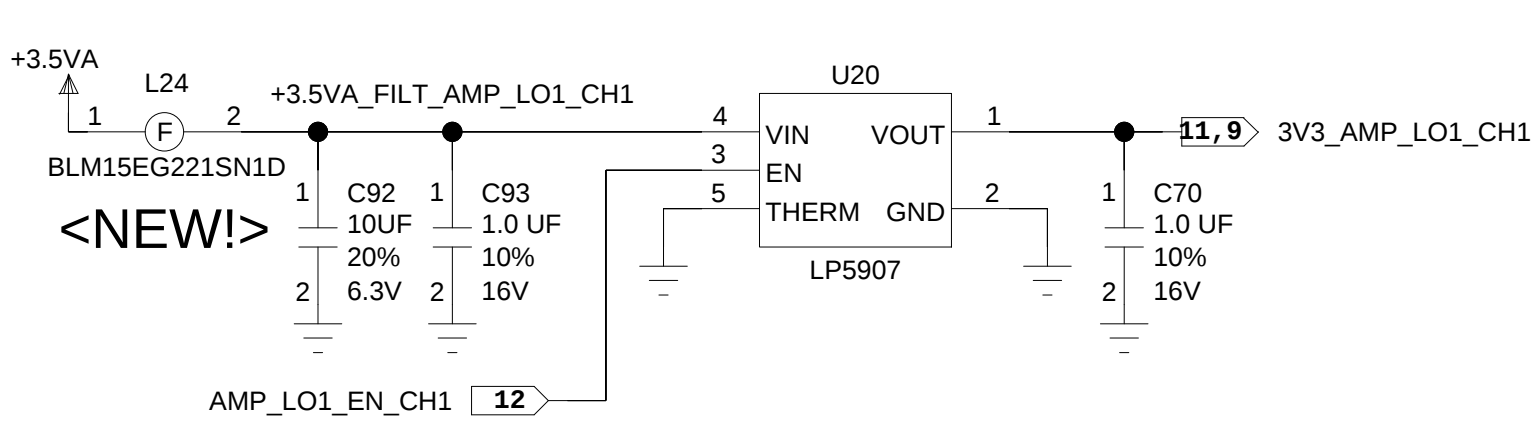
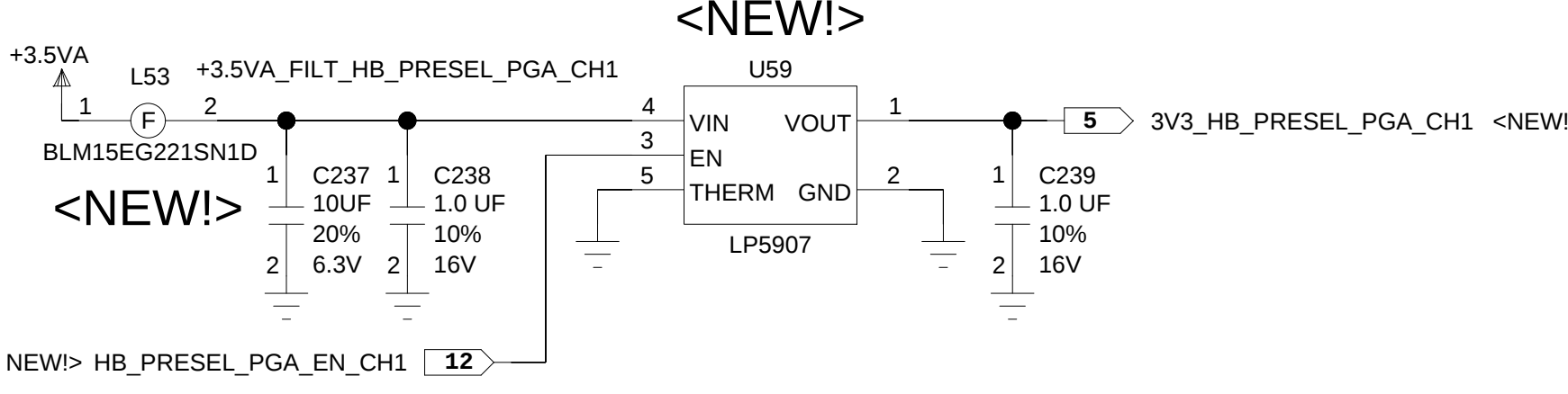
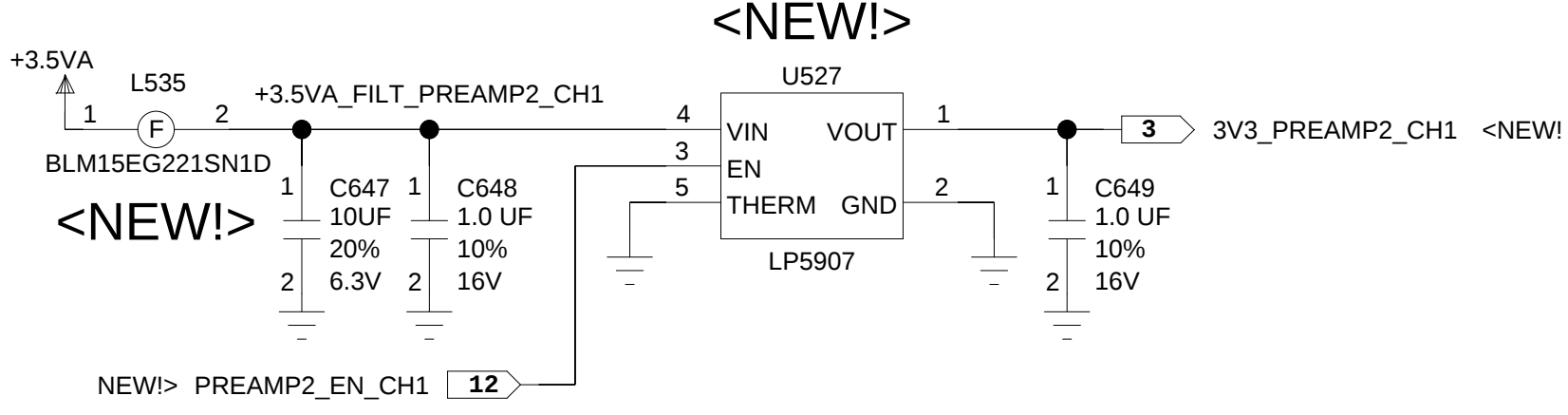
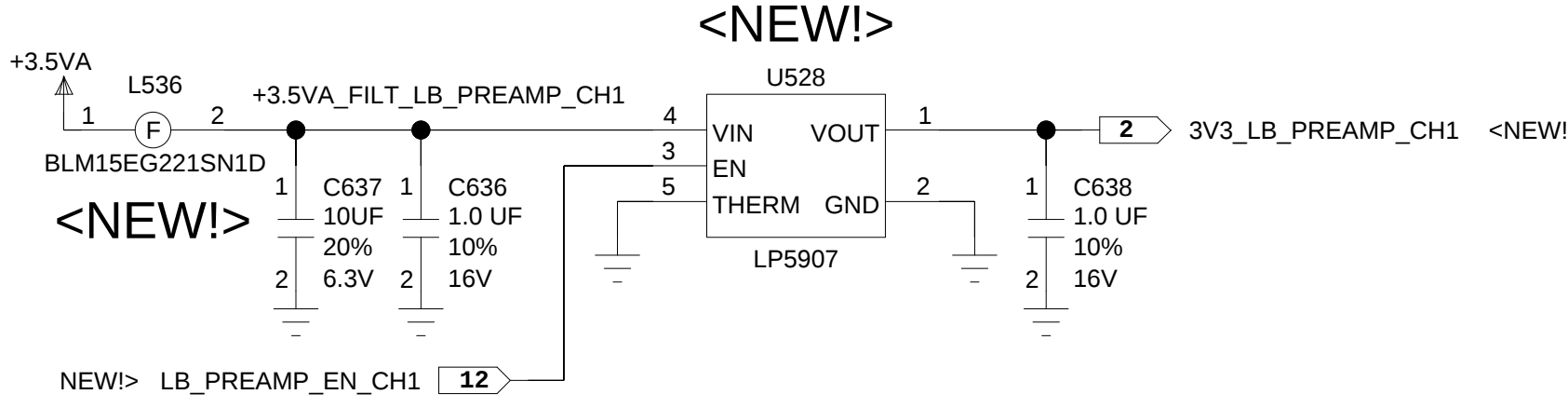
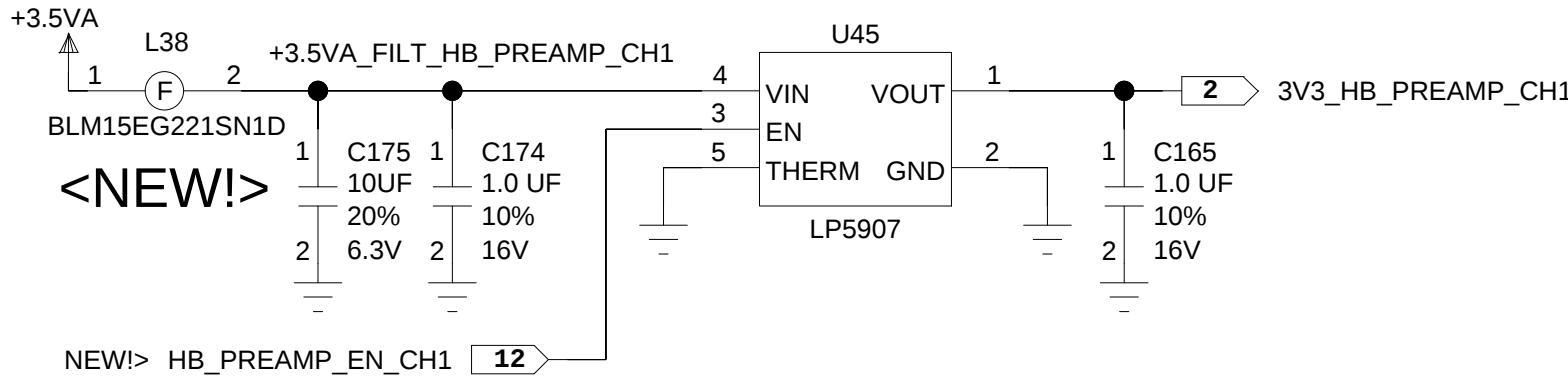
LB SW: 3.72V to 3.3V



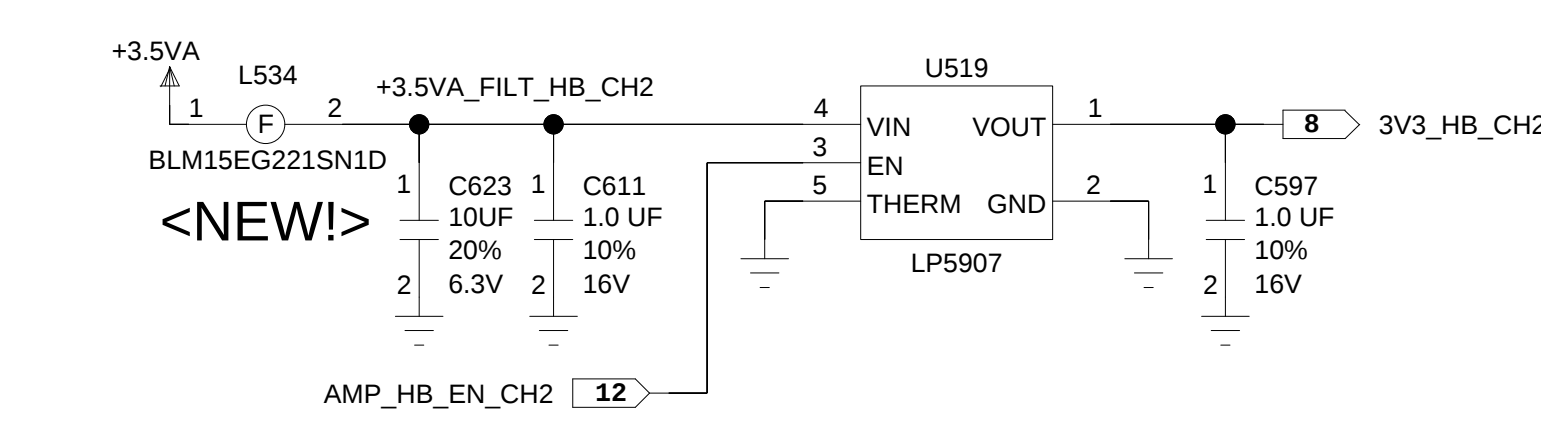
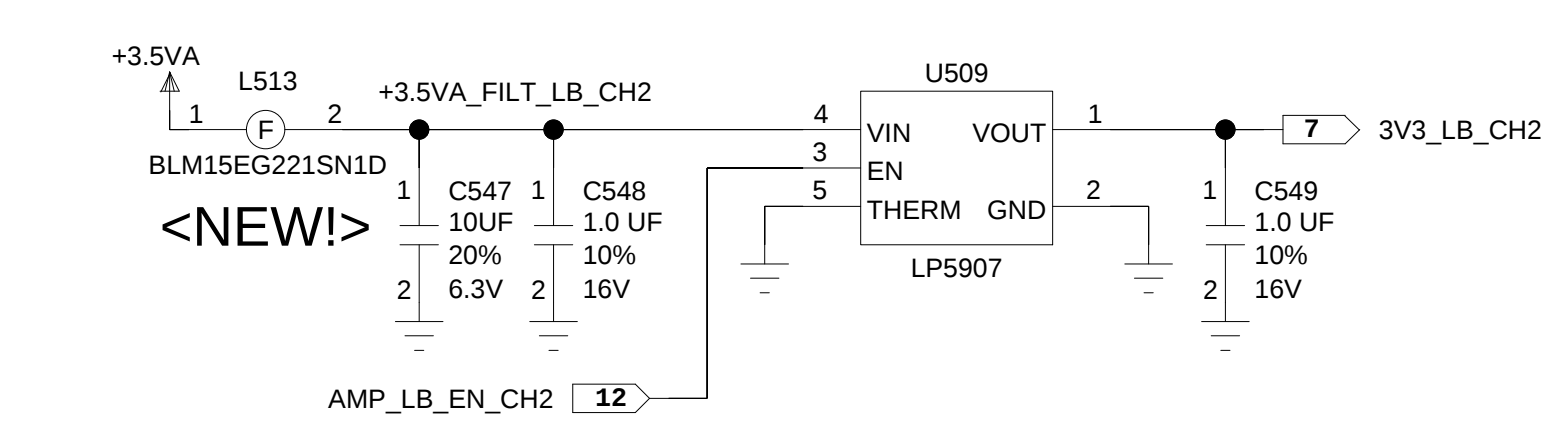
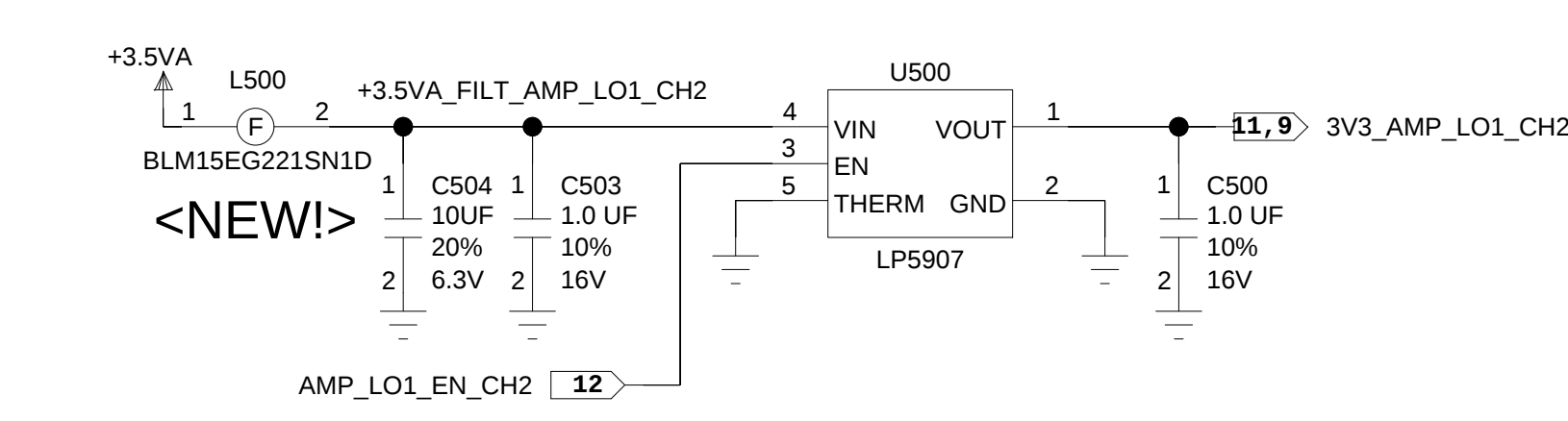
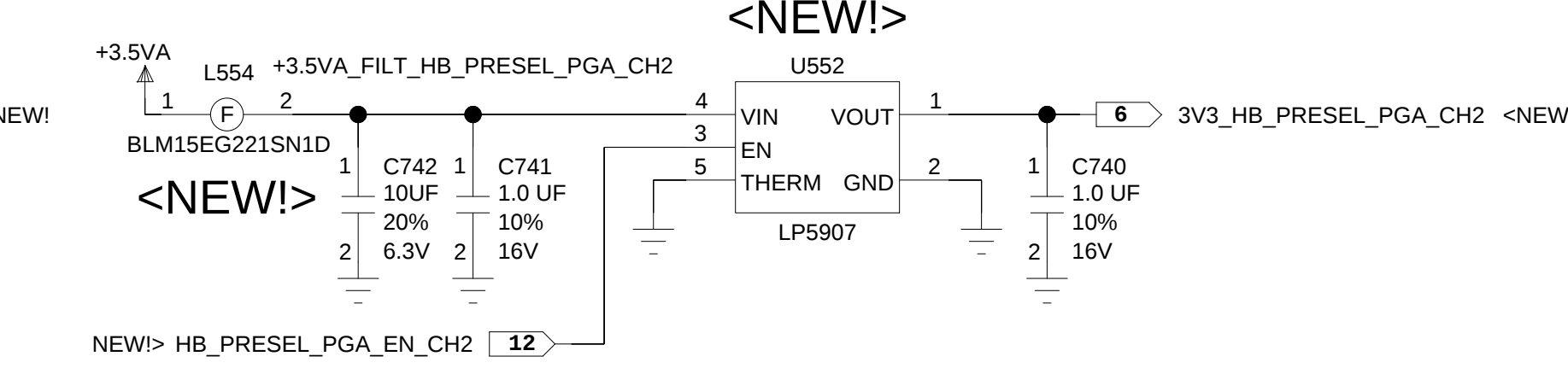
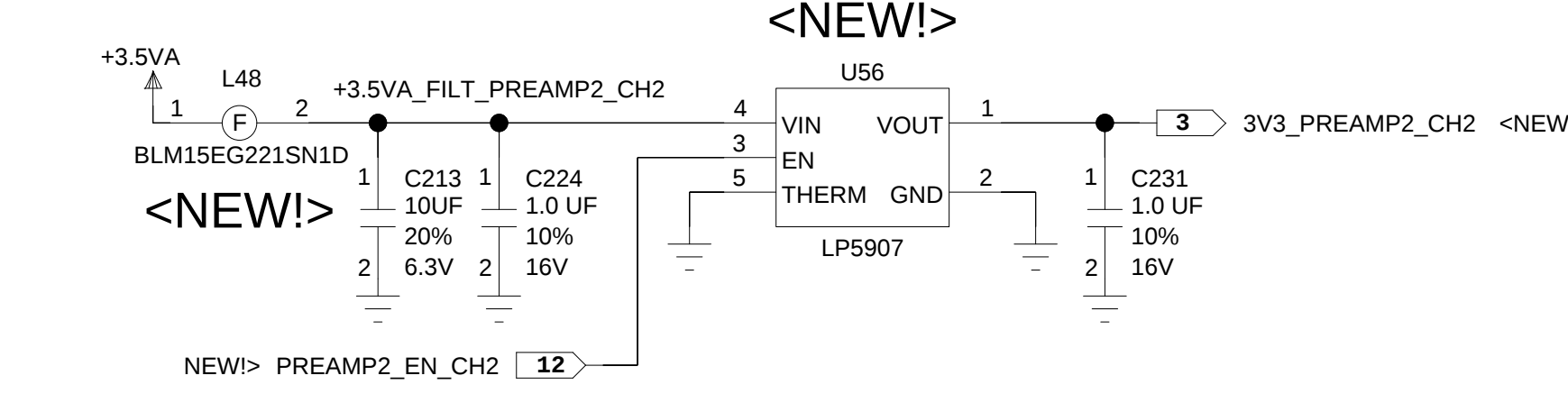
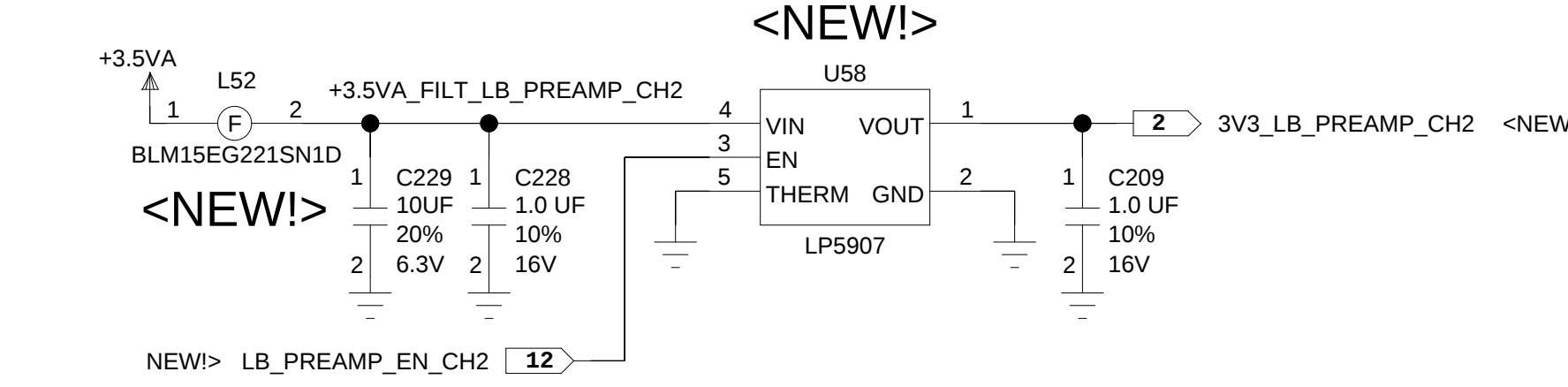
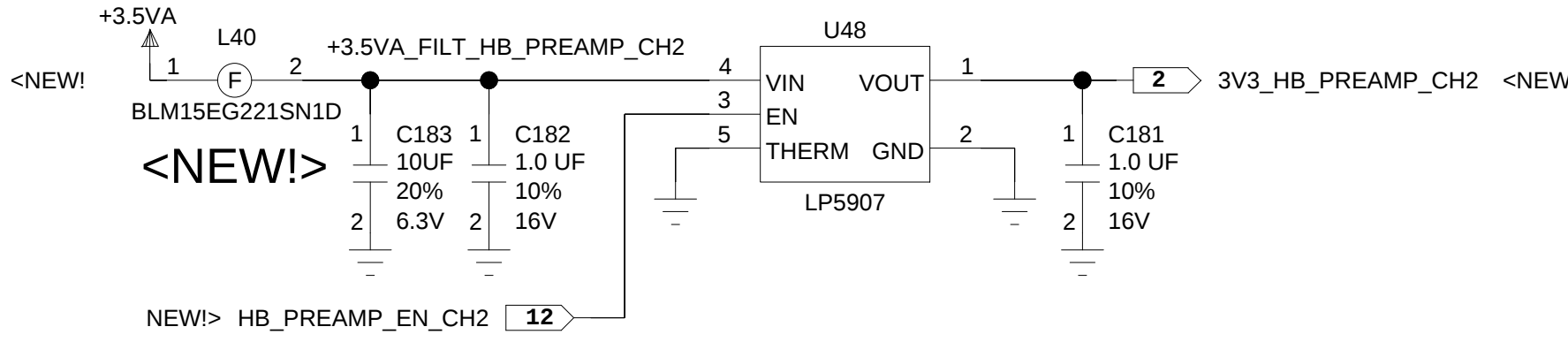
CPLD LDO: 5V to 1.8V



CH1 LDOs w/EN: 3.72V to 3.3V



CH2 LDOs w/EN: 3.72V to 3.3V



13-Power Supply

TWINRX USRP RF BOARD

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