

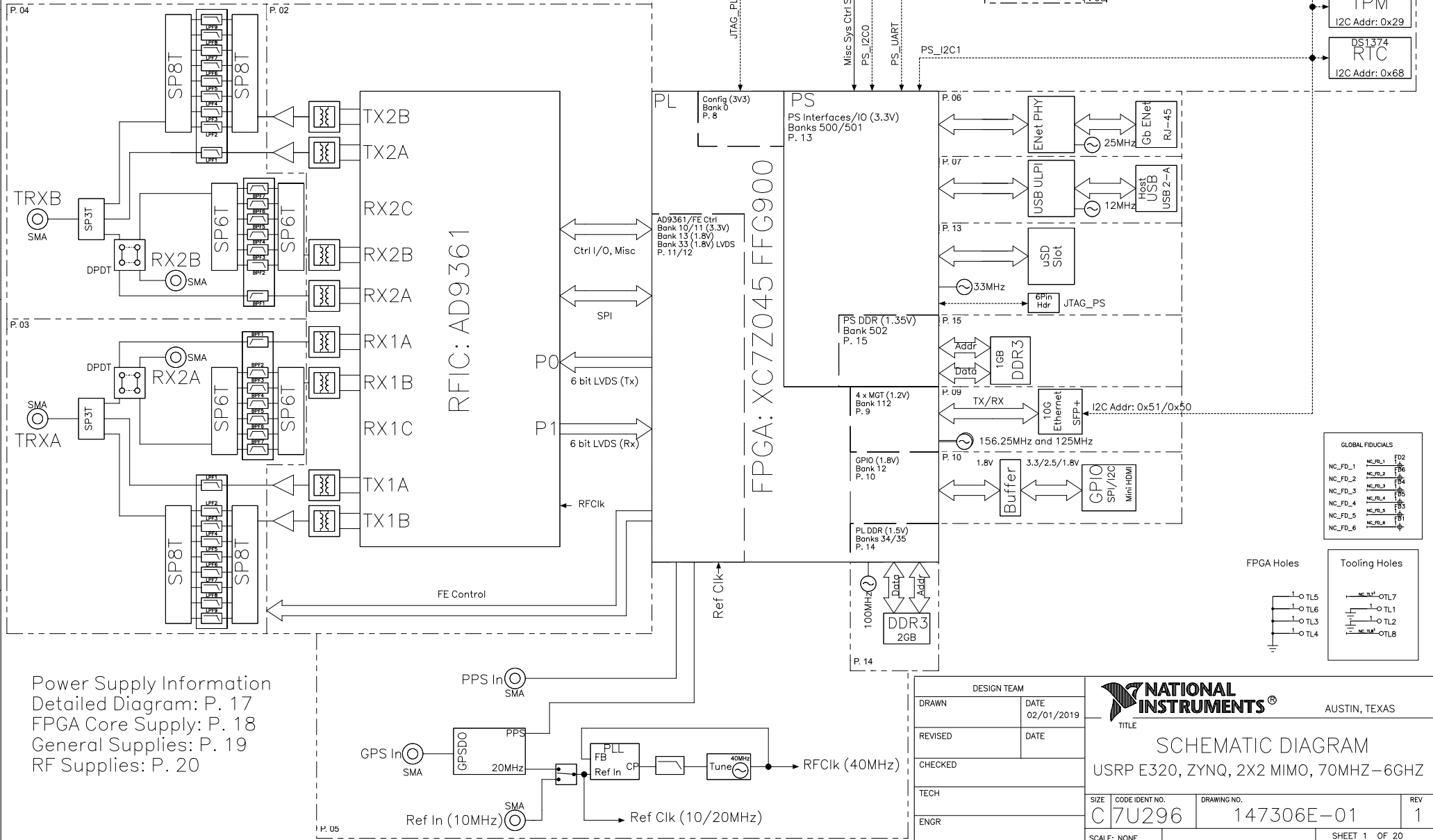
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This schematic is for general understanding of the E320 hardware and may not be up to date with the latest hardware changes.

Filter Plan

BP1: HFCN-2700A+
BP2: LFCN-400+
BP3: HFCN-440+ / LFCN-530+
BP4: HFCN-650+ / LFCN-1000+
BP5: HFCN-1100+ / LFCN-1575+
BP6: HFCN-1600+ / LFCN-2250+
BP7: HFCN-2100+ / LFCN-2850+

LP1: LFCN-5850+
LP2: LFCN-2750+
LP3: LFCN-1700+
LP4: LFCN-1000+
LP5: LFCN-575+
LP6: LFCN-400+
LP7: LFCN-225+
LP8: LFCN-160+
LP9: LFCN-80+



Power Supply Information
Detailed Diagram: P. 17
FPGA Core Supply: P. 18
General Supplies: P. 19
RF Supplies: P. 20

DESIGN TEAM	
DRAWN	DATE
REVISED	DATE
CHECKED	
TECH	
ENGR	



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AUSTIN, TEXAS

TITLE

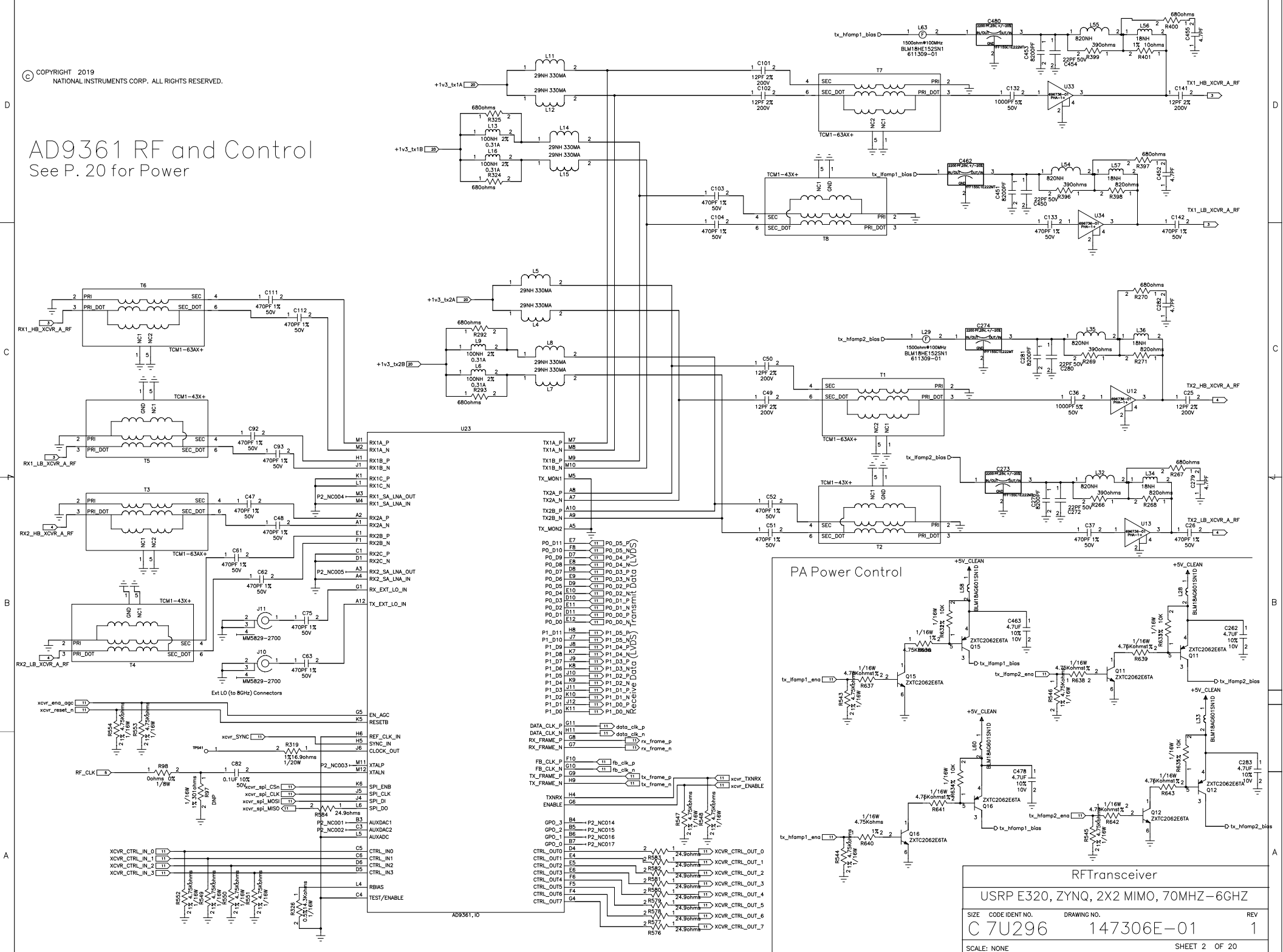
SCHEMATIC DIAGRAM

USRP E320, ZYNQ, 2X2 MIMO, 70MHZ-6GHZ

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	7U296	147306E-01	1

AD9361 RF and Control

See P. 20 for Power



RFTransceiver			
USRP E320, ZYNQ, 2X2 MIMO, 70MHZ-6GHZ			
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C 7U296		147306E-01	1
SCALE: NONE		SHEET 2 OF 20	

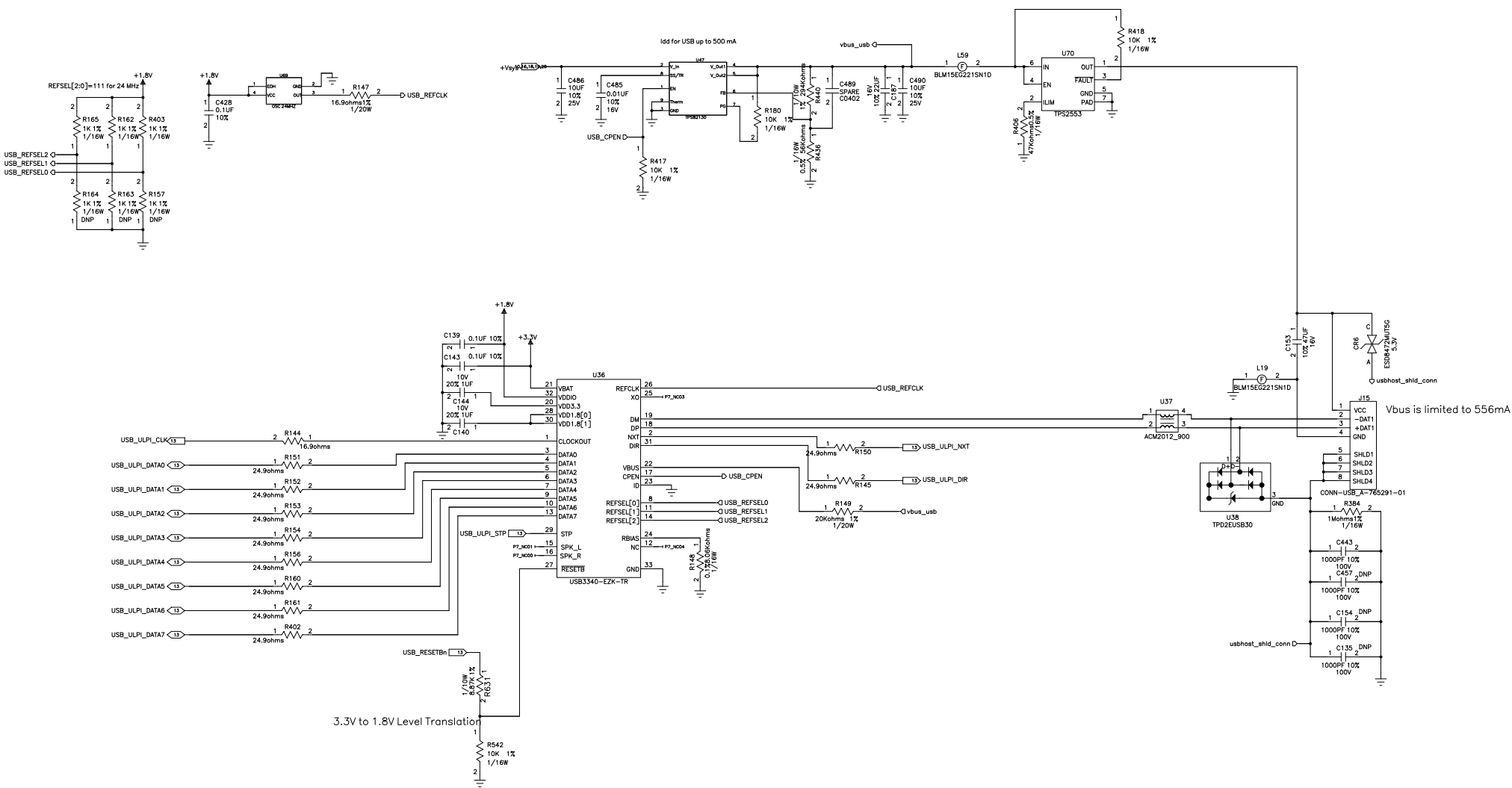


RF Ch A Front-End			
USRP E320, ZYNQ, 2X2 MIMO, 70MHZ-6GHZ			
C	CODE IDENT NO.	DRAWING NO.	REV
SIZE	7U296	147306E-01	1
SCALE: NONE			SHEET 3 OF 20

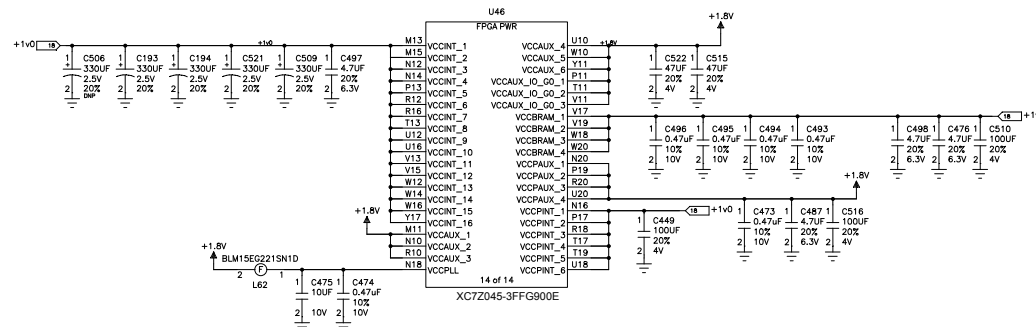


SCALE: NONE SHEET 4 OF 20

Clocking			
USRP E320, ZYNQ, 2X2 MIMO, 70MHZ-6GHZ			
SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	7U296	147306E-01	1
SCALE: NONE			SHEET 5 OF 20

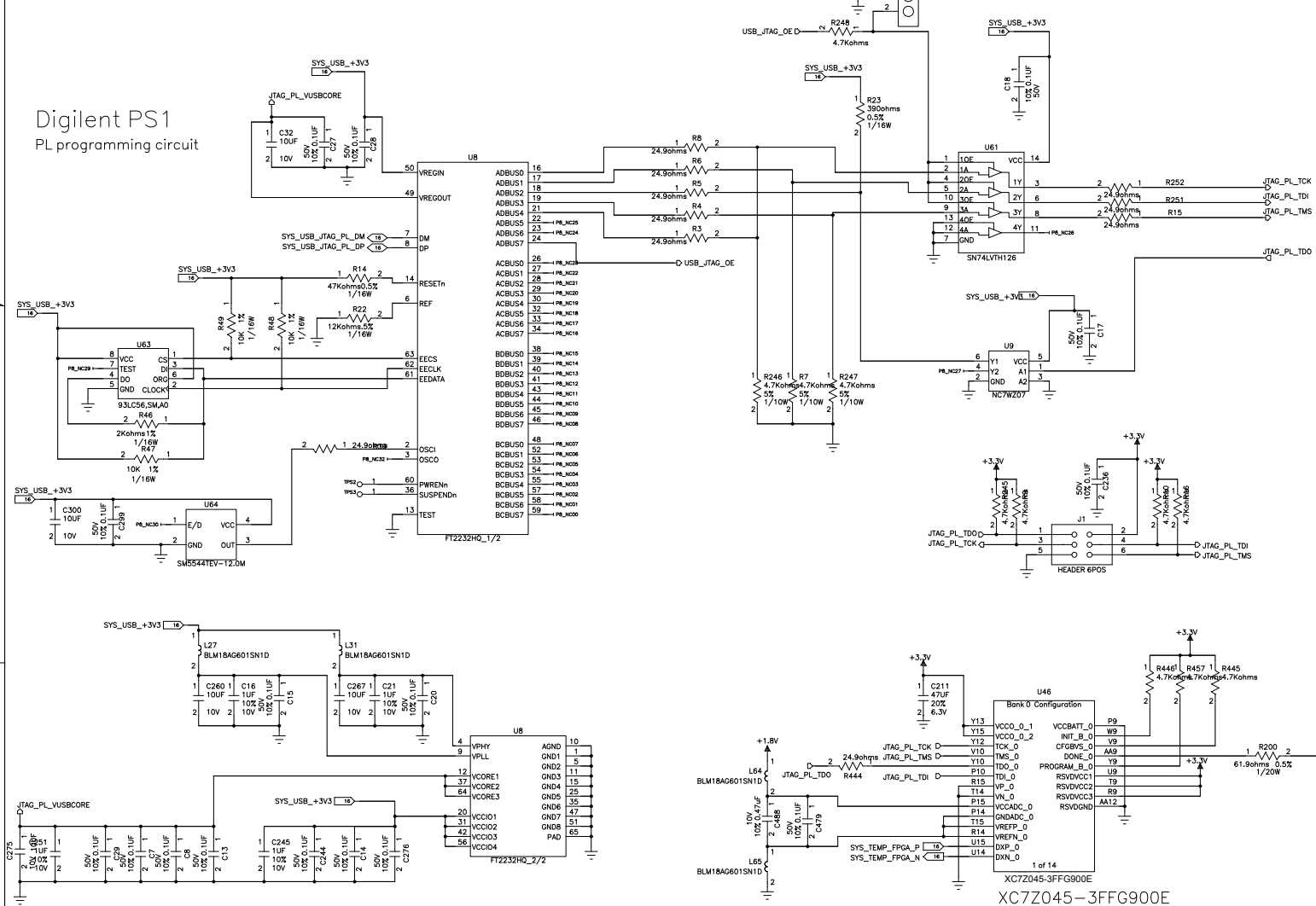


USB-Host			
USRP E320, ZYNQ, 2X2 MIMO, 70MHZ-6GHZ			
SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	7U296	147306E-01	1
SCALE: NONE		SHEET 7 OF 20	

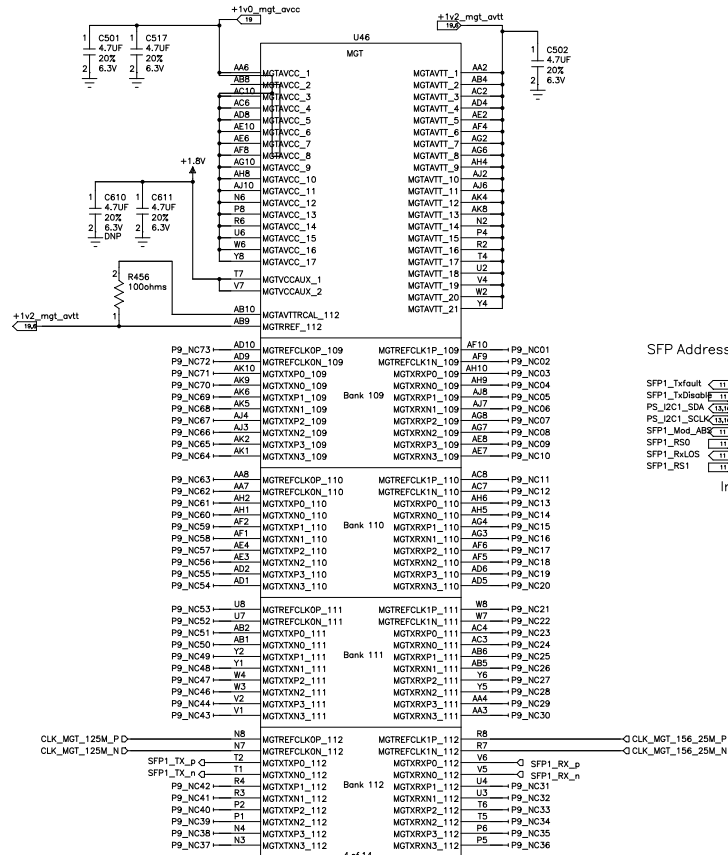


Direct JTAG:
Short the OE jumper (To the left) to disable Digilent programmer

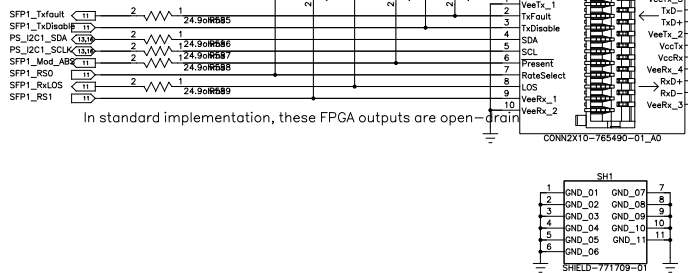
Digilent PS1
PL programming circuit



A1	GND_1	GND_80	J27
A11	GND_2	GND_81	J7
A21	GND_3	GND_82	K14
AA1	GND_4	GND_83	K4
AA10	GND_5	GND_84	L11
AA11	GND_6	GND_85	M1
AA21	GND_7	GND_86	M2
AB1	GND_8	GND_87	M14
AB11	GND_9	GND_88	M18
AB18	GND_10	GND_89	M28
AB28	GND_11	GND_90	M3
AB3	GND_12	GND_91	M3
AB7	GND_13	GND_92	M6
AC1	GND_14	GND_93	M4
AC11	GND_15	GND_94	M5
AC15	GND_16	GND_95	M7
AC25	GND_17	GND_96	M8
AC5	GND_18	GND_97	M9
AD11	GND_19	GND_98	N1
AD12	GND_20	GND_99	N11
AD23	GND_21	GND_100	N15
AD22	GND_22	GND_101	N13
AD7	GND_23	GND_102	N17
AE1	GND_24	GND_103	N19
AE11	GND_25	GND_104	N5
AE18	GND_26	GND_105	N25
AE29	GND_27	GND_106	N9
AE5	GND_28	GND_107	P12
AE9	GND_29	GND_108	P18
AF11	GND_30	GND_109	P16
AF16	GND_31	GND_110	P22
AF26	GND_32	GND_111	P22
AF3	GND_33	GND_112	P3
AF7	GND_34	GND_113	P7
AG1	GND_35	GND_114	R1
AG11	GND_36	GND_115	R11
AG23	GND_37	GND_116	R13
AG3	GND_38	GND_117	R17
AG5	GND_39	GND_118	R19
AG9	GND_40	GND_119	R29
AH11	GND_41	GND_120	R5
AH20	GND_42	GND_121	T10
AH3	GND_43	GND_122	T12
AH30	GND_44	GND_123	T16
AH7	GND_45	GND_124	T18
AJ1	GND_46	GND_125	T20
AJ11	GND_47	GND_126	T26
AJ27	GND_48	GND_127	T8
AJ7	GND_49	GND_128	T3
AJ9	GND_50	GND_129	U1
AK11	GND_51	GND_130	U11
AK14	GND_52	GND_131	U13
AK24	GND_53	GND_132	U17
AK3	GND_54	GND_133	U19
AK7	GND_55	GND_134	U23
B18	GND_56	GND_135	U5
B28	GND_57	GND_136	U5
B3	GND_58	GND_137	V14
B5	GND_59	GND_138	V18
B8	GND_60	GND_139	V16
C15	GND_61	GND_140	V20
C25	GND_62	GND_141	V3
C5	GND_63	GND_142	V30
D2	GND_64	GND_143	V8
D22	GND_65	GND_144	W1
D29	GND_66	GND_145	W11
E19	GND_67	GND_146	W15
E29	GND_68	GND_147	W17
F16	GND_69	GND_148	W17
F26	GND_70	GND_149	W19
F6	GND_71	GND_150	W27
G13	GND_72	GND_151	W5
G23	GND_73	GND_152	Y14
G3	GND_74	GND_153	Y16
H10	GND_75	GND_154	Y18
H20	GND_76	GND_155	Y24
H30	GND_77	GND_156	Y3
J17	GND_78	GND_157	Y7
	GND_79	GND_158	Y7

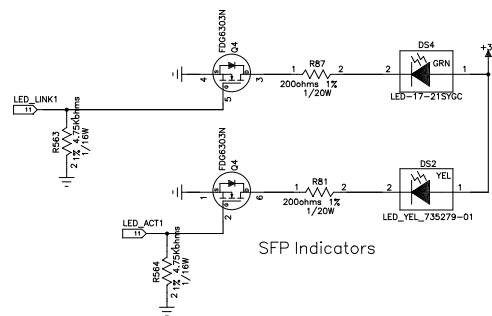


SFP Address: 0x51/0x50



In standard implementation, these FPGA outputs are open-drain

Shield/Shell for SFP

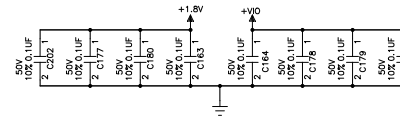
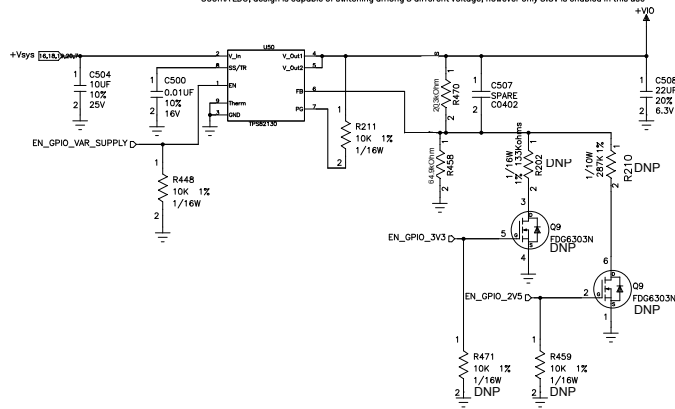


SFP Indicators

SFP			
USRP E320, ZYNQ, 2X2 MIMO, 70MHZ-6GHZ			
SIZE	CODE IDENT NO.	DRAWING NO.	REV
C 7U296	147306E-01		1
SCALE: NONE			SHEET 9 OF 20

Variable GPIO Power Supply

500mA LDO, design is capable of switching among 3 different voltage, however only 3.3V is enabled in this use



GPIO Logic Levels

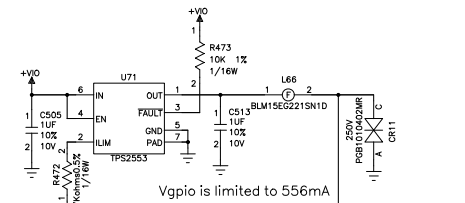
Input
VIH: 2V
VIL: 0.8V

Output
IOH: 12mA @ nominal 3.3V
IOL: 12mA @ nominal GND

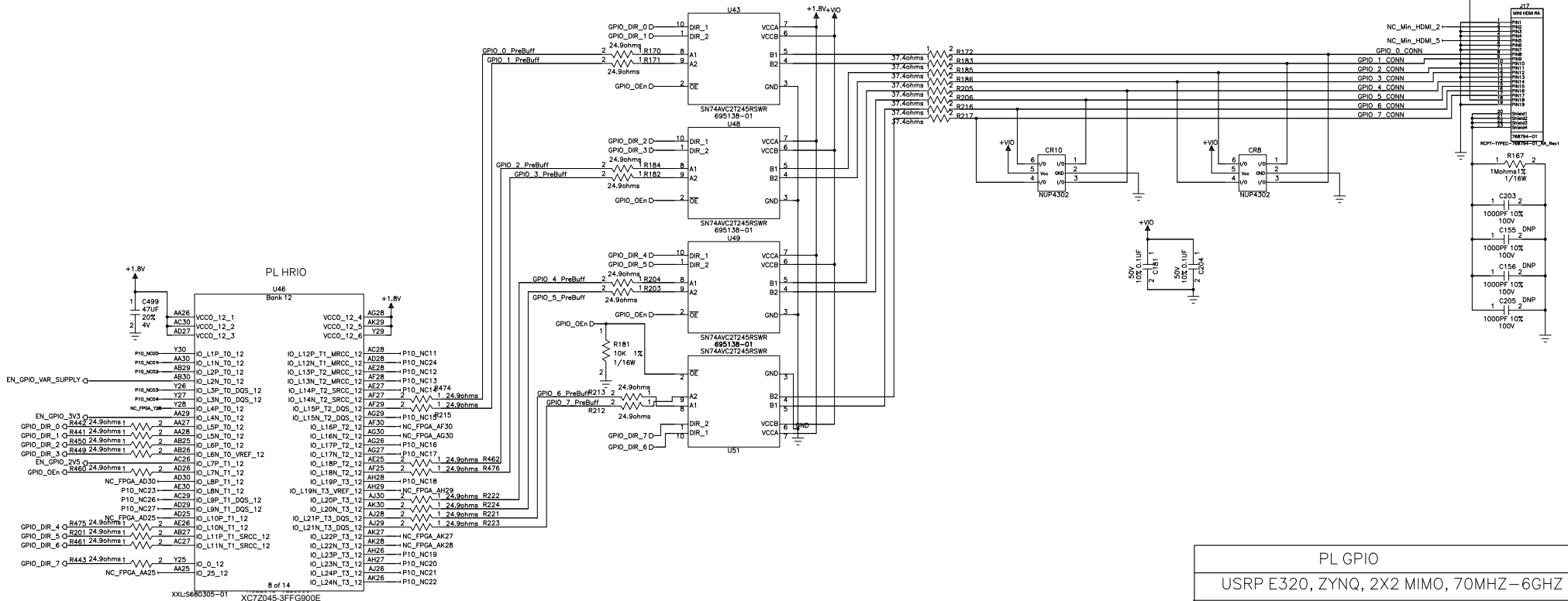
Absolute Max Ratings:

Pins Configured for Output
-0.5V < Vgpio < 3.7V

Pins Configured for Input
-0.5V < Vgpio < 4.5V



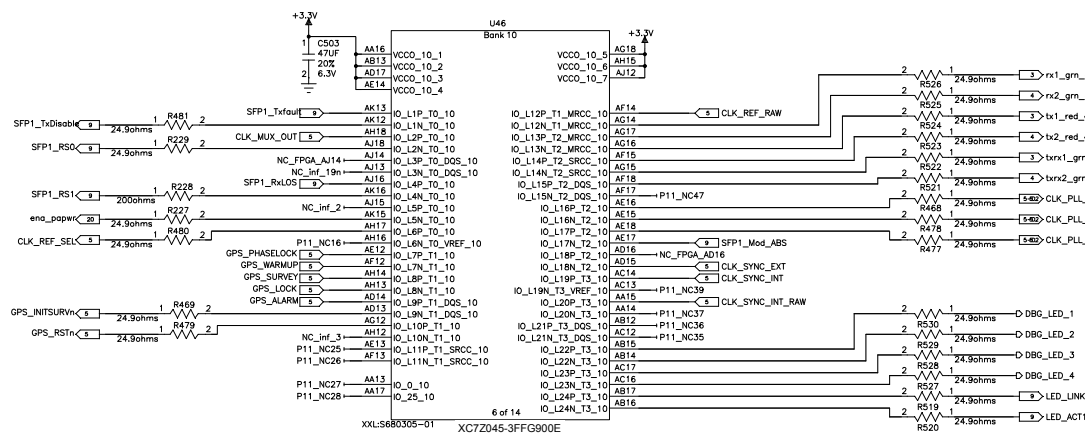
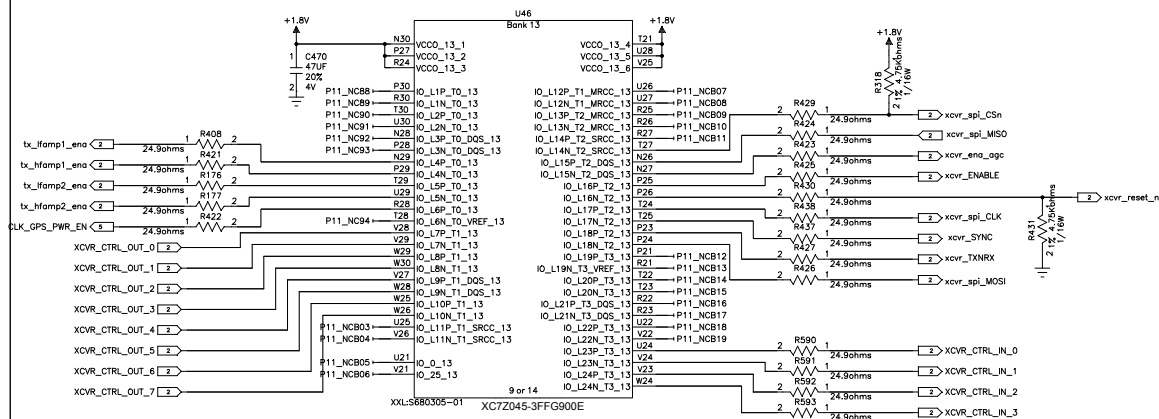
Vgpio is limited to 556mA



PL GPIO			
USRP E320, ZYNQ, 2X2 MIMO, 70MHZ-6GHZ			
SIZE	CODE IDENT NO.	DRAWING NO.	REV
C 7U296		147306E-01	1
SCALE: NONE		SHEET 10 OF 20	

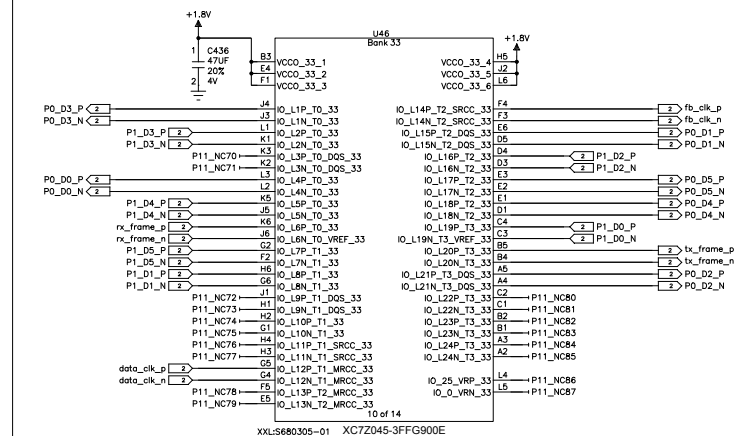
PL HRIO

ADF4002 SPI
Front End PA Power Enable
Front End LED Control
GPS Power Enable
AD9361 SPI
Misc GPS IO
Misc SFP IO

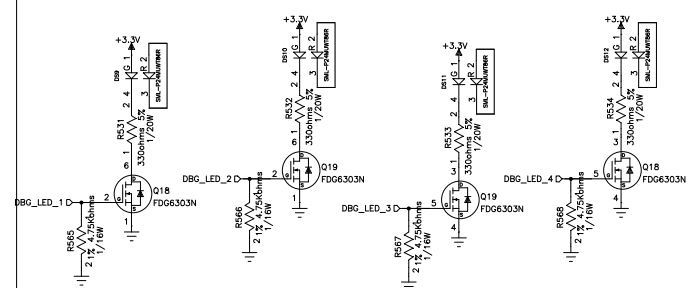


PL HPIO

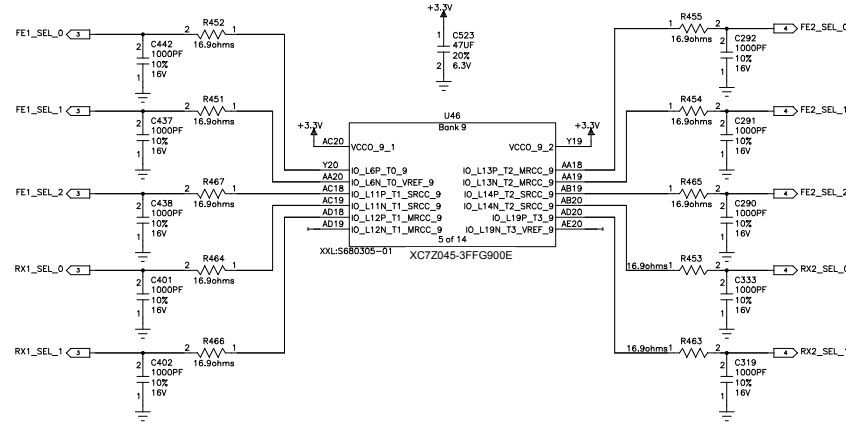
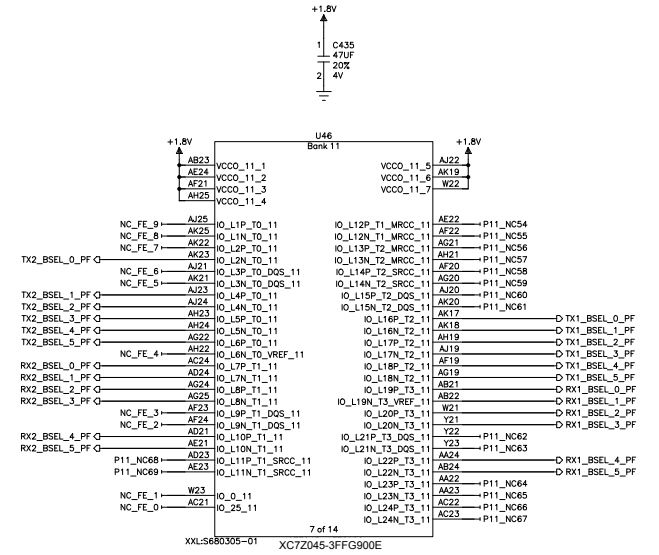
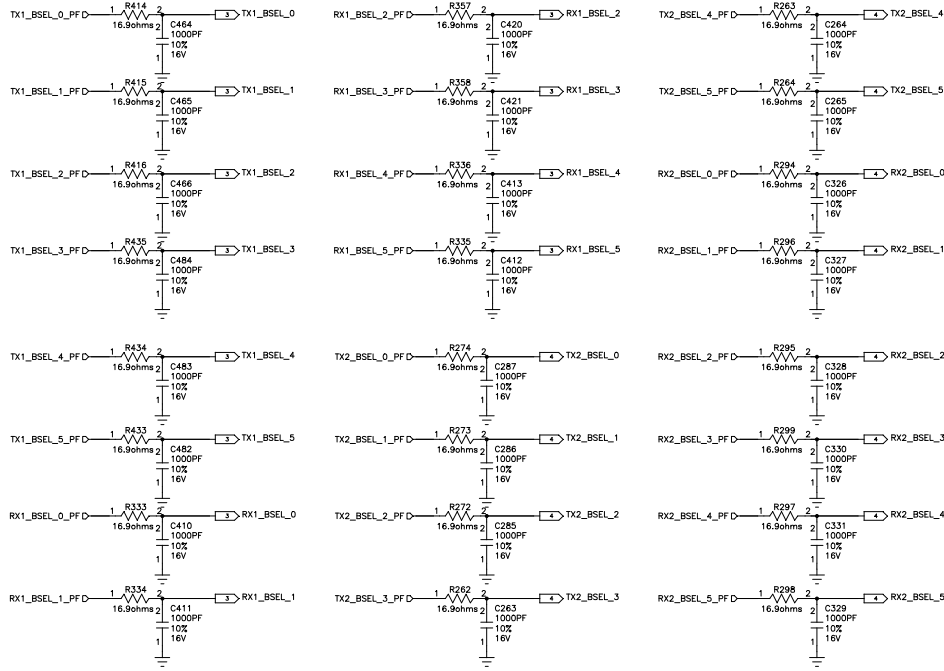
AD9361 LVDS IC

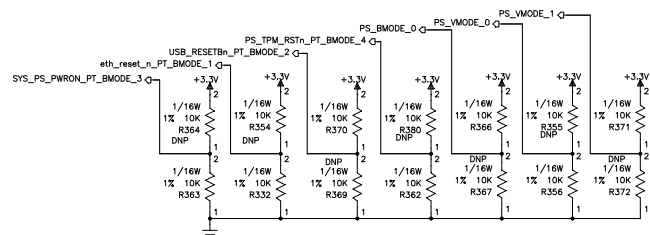
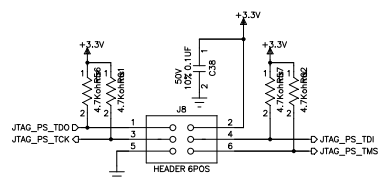


Debug LEDs



PL 10			
USRP E320, ZYNQ, 2X2 MIMO, 70MHZ-6GHZ			
SIZE	CODE IDENT. NO.	DRAWING NO.	REV
C	7U296	147306E-01	1
SCALE: NONE		SHEET 11 OF 20	

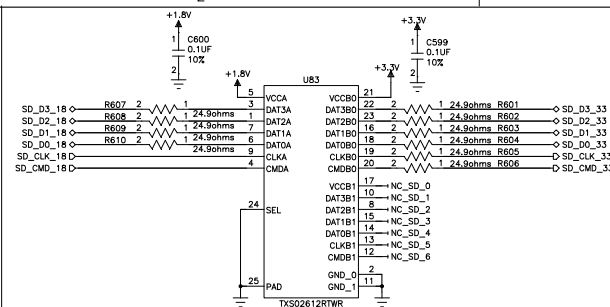
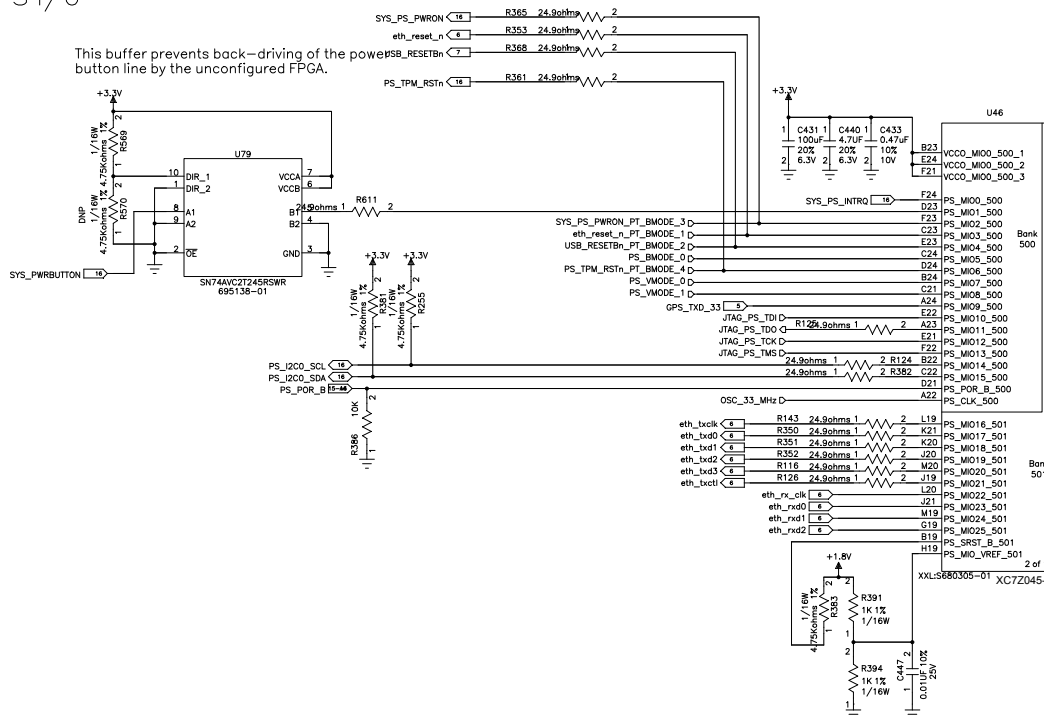




Boot Mode Config (See table 6–4 from UG585):
SD Card Boot Device
Independent JTAG Mode
PLL Enabled
3.3V Bank Voltage (500)/1.8V Bank Voltage (501)

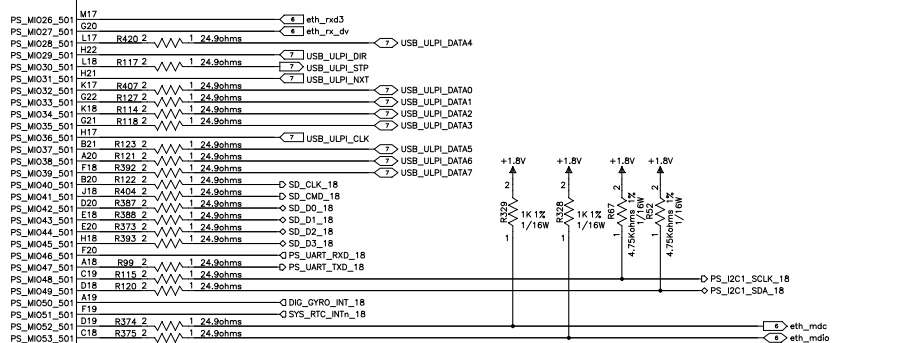
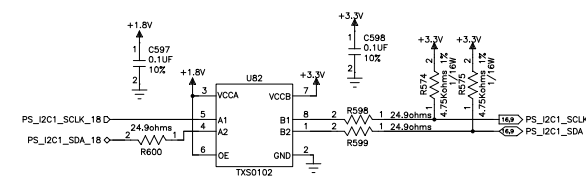
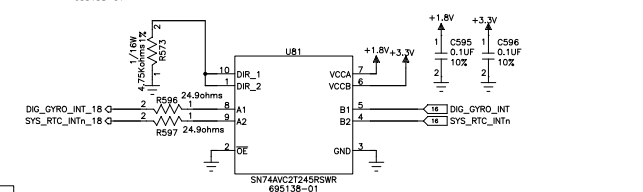
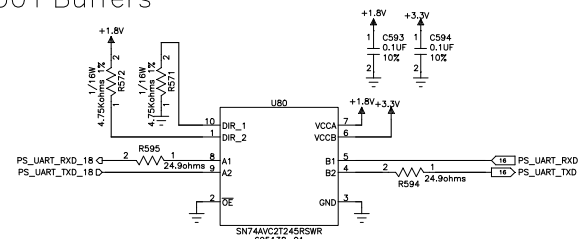
PS I/O

This buffer prevents back-driving of the power button line by the unconfigured FPGA.

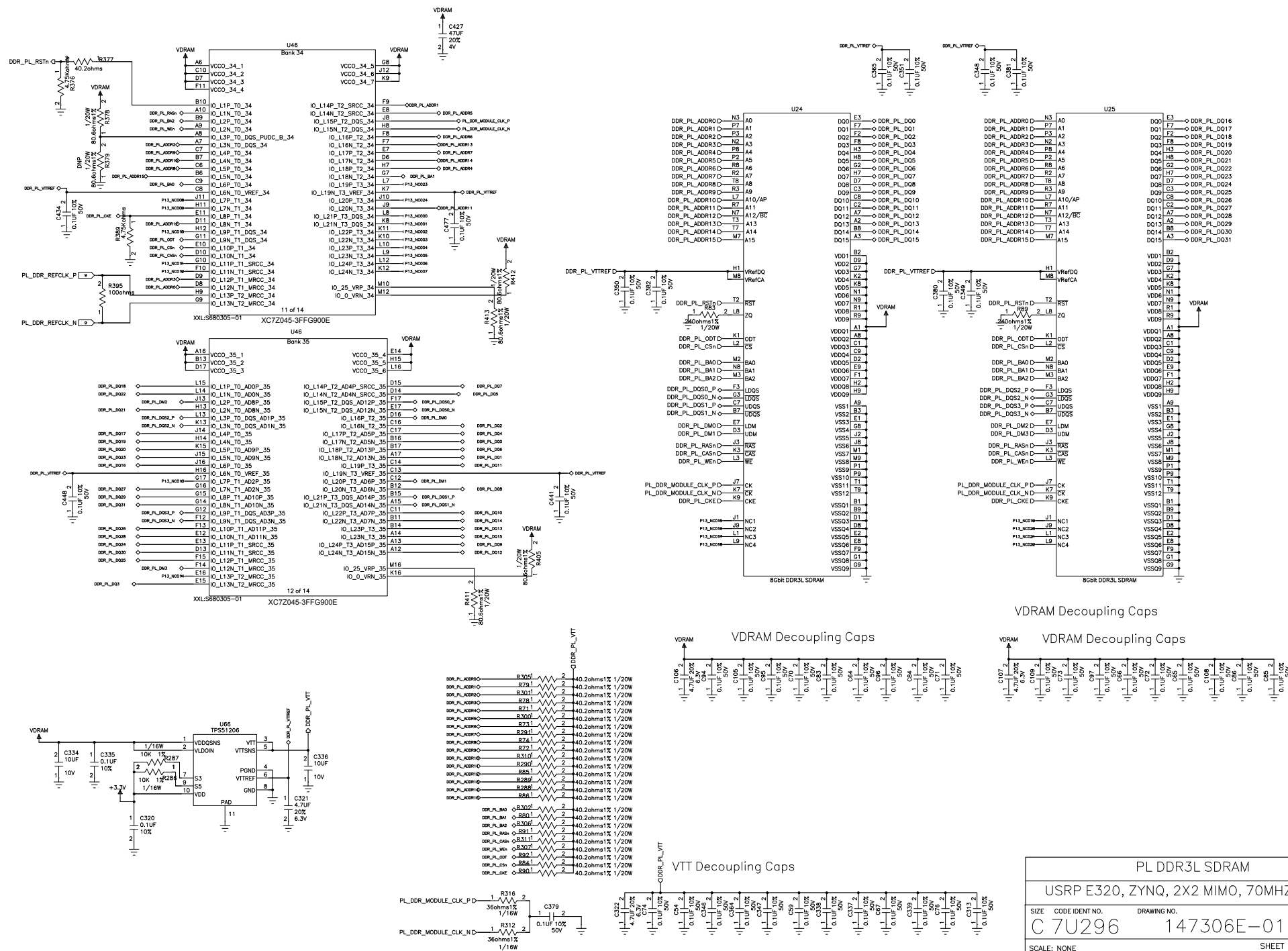


SD/Voltage Translator

Bank 501 Buffers

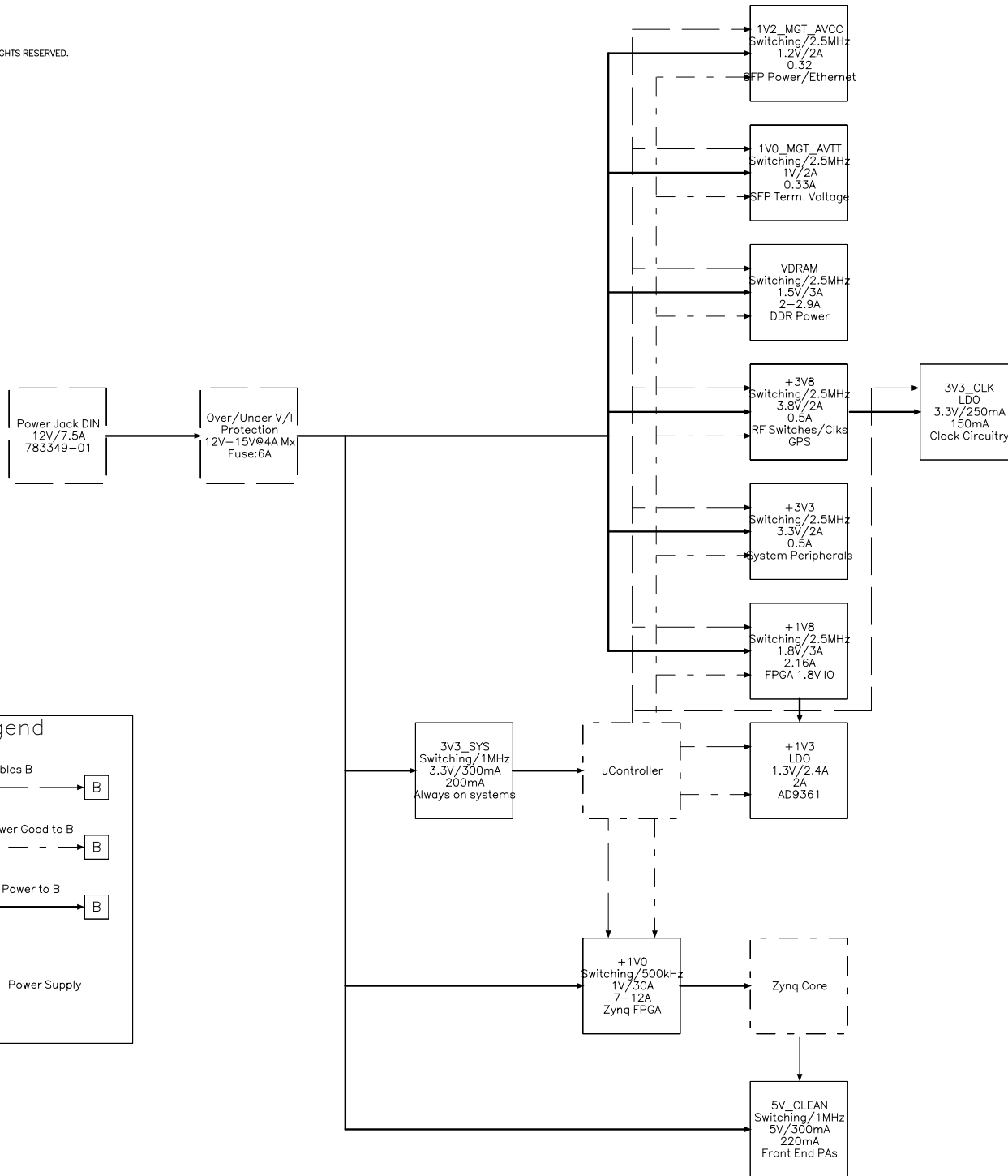
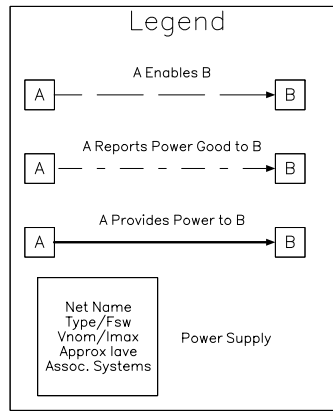


PS IO			
USRP E320, ZYNQ, 2X2 MIMO, 70MHZ-6GHZ			
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SCALE: NONE		SHEET 13 OF 20	



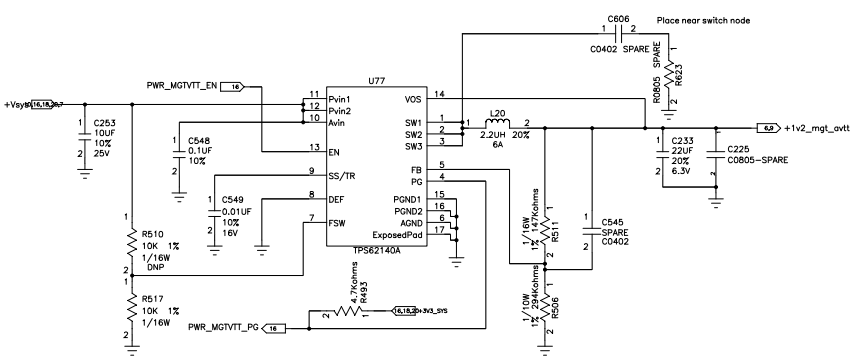
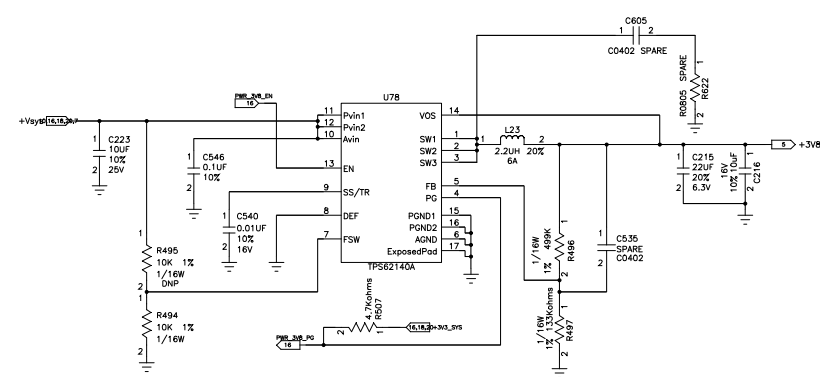
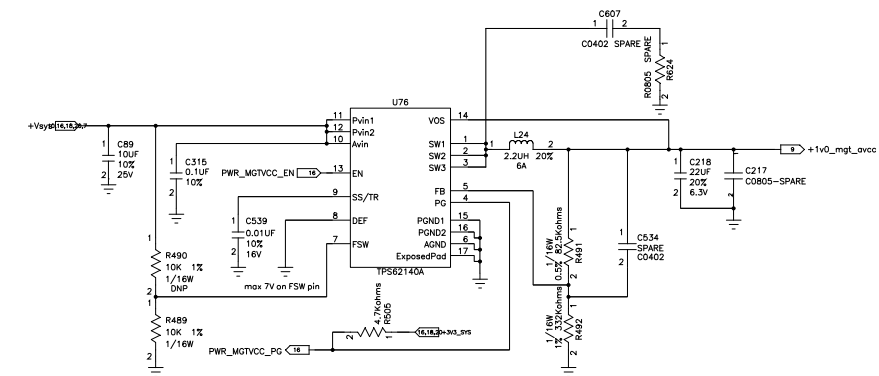
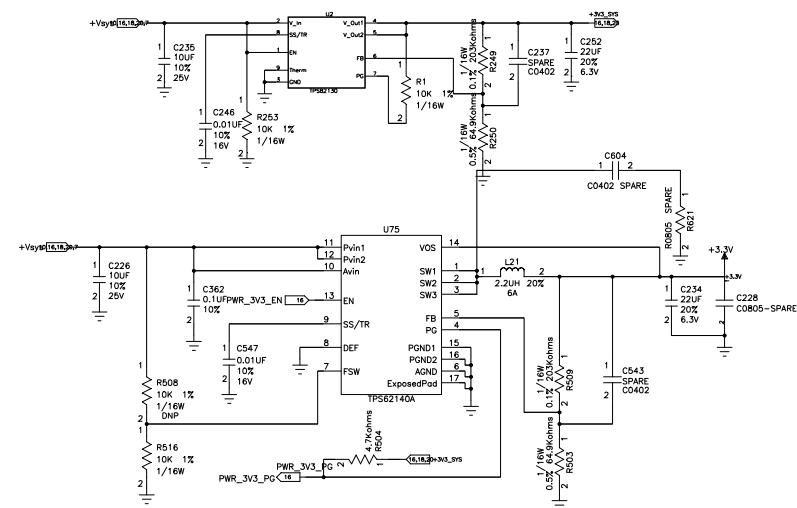
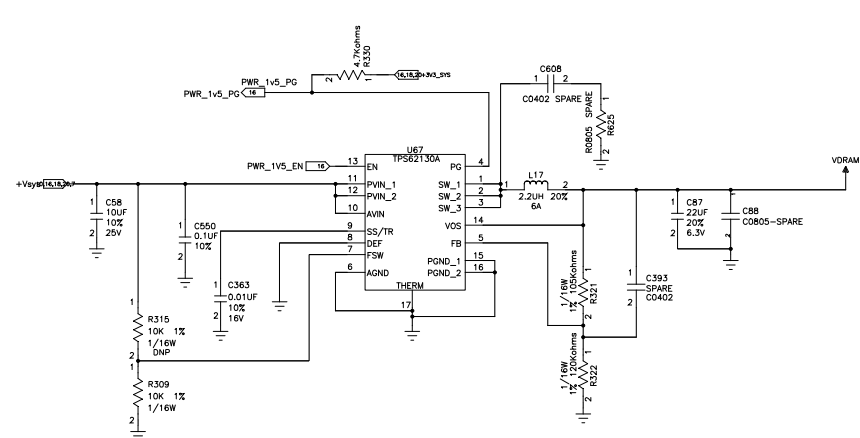
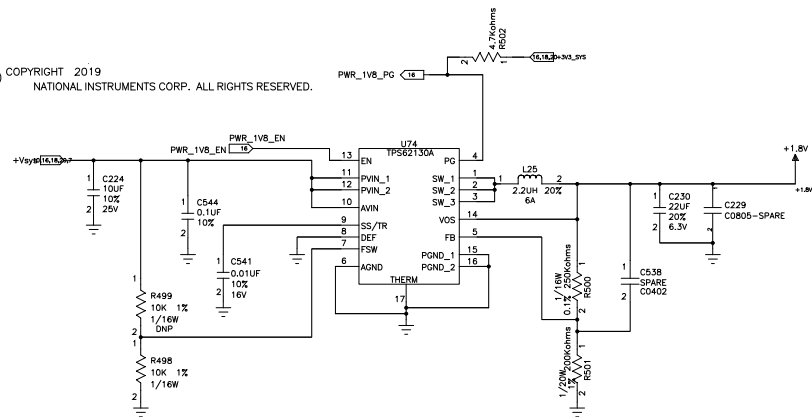


PS DDR3L SDRAM			
USRP E320, ZYNQ, 2X2 MIMO, 70MHZ-6GHZ			
SIZE C	CODE IDENT NO. 7U296	DRAWING NO. 147306E-01	REV 1
SCALE: NONE		SHEET 15 OF 20	

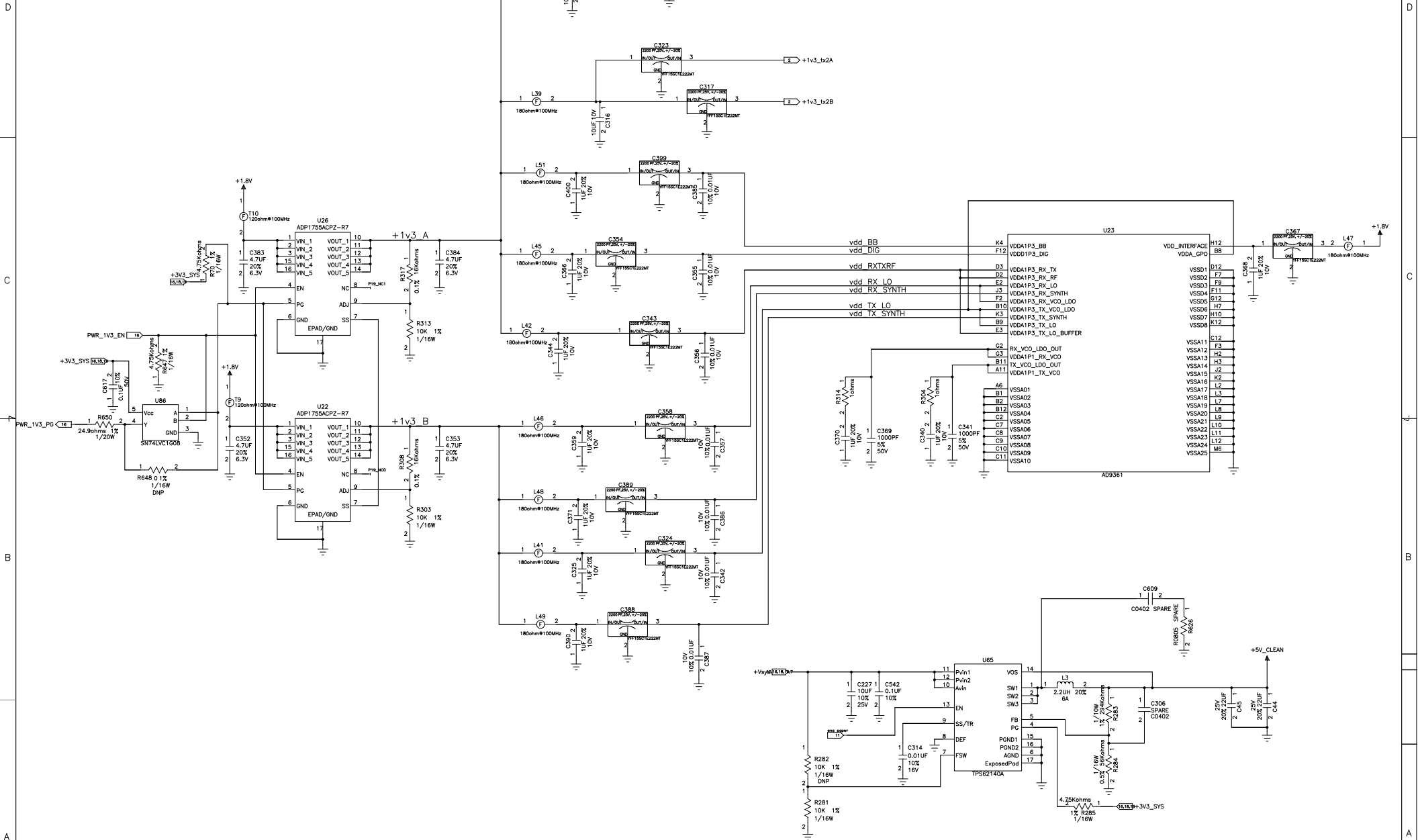


Power Supply Diagram/Info			
USRP E320, ZYNQ, 2X2 MIMO, 70MHZ-6GHZ			
SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	7U296	147306E-01	1
SCALE: NONE		SHEET 17 OF 20	

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General Purpose Power Rails			
USRP E320, ZYNQ, 2X2 MIMO, 70MHZ-6GHZ			
SIZE	CODE/IDENT NO.	DRAWING NO.	REV
C	7U296	147306E-01	1
SCALE: NONE		SHEET 19 OF 20	



Xcvr Power			
USRP E320, ZYNQ, 2X2 MIMO, 70MHZ-6GHZ			
SIZE	CODE/IDENT NO.	DRAWING NO.	REV
C 7U296		147306E-01	1
SCALE: NONE		SHEET 20 OF 20	