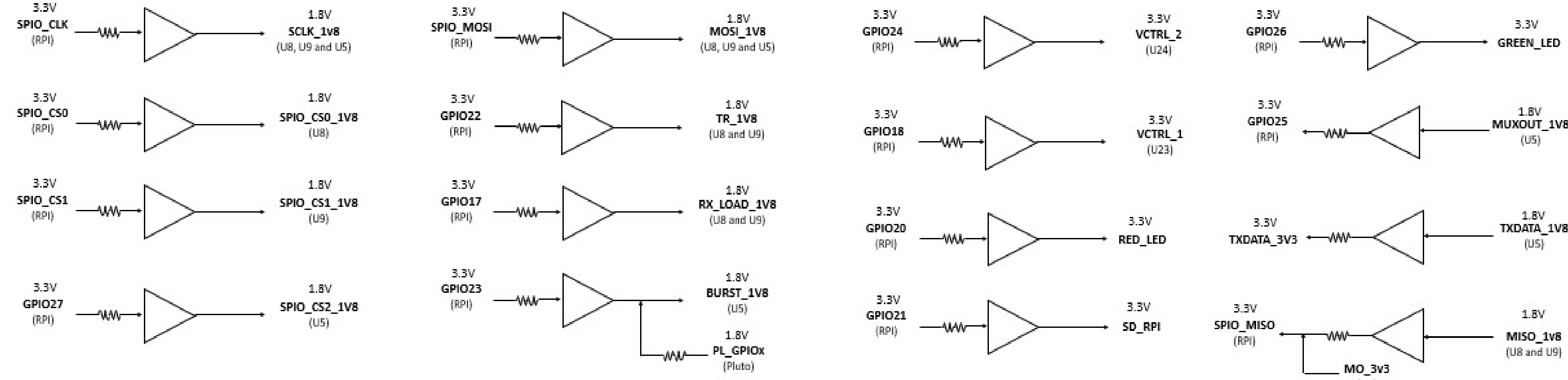
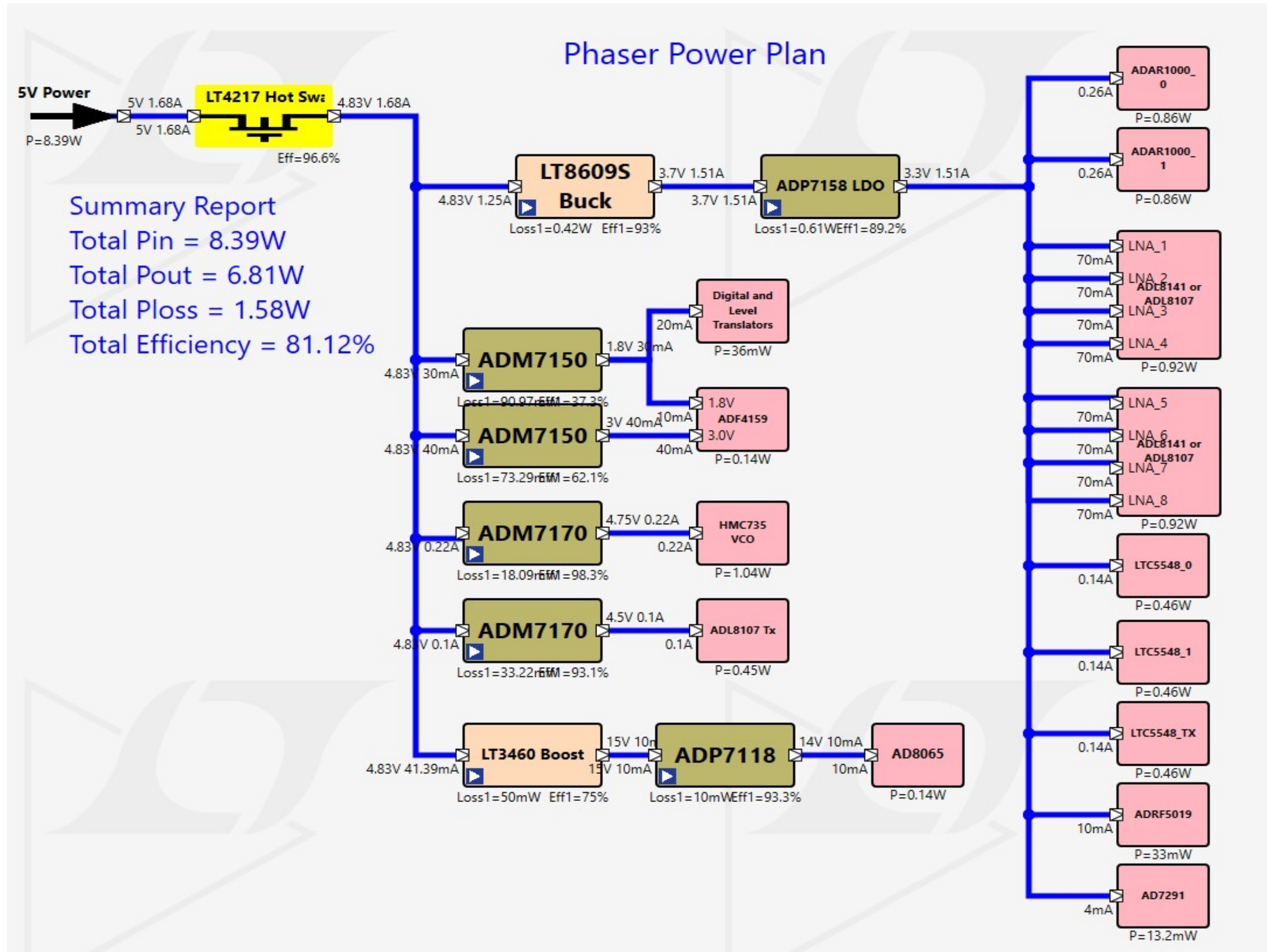
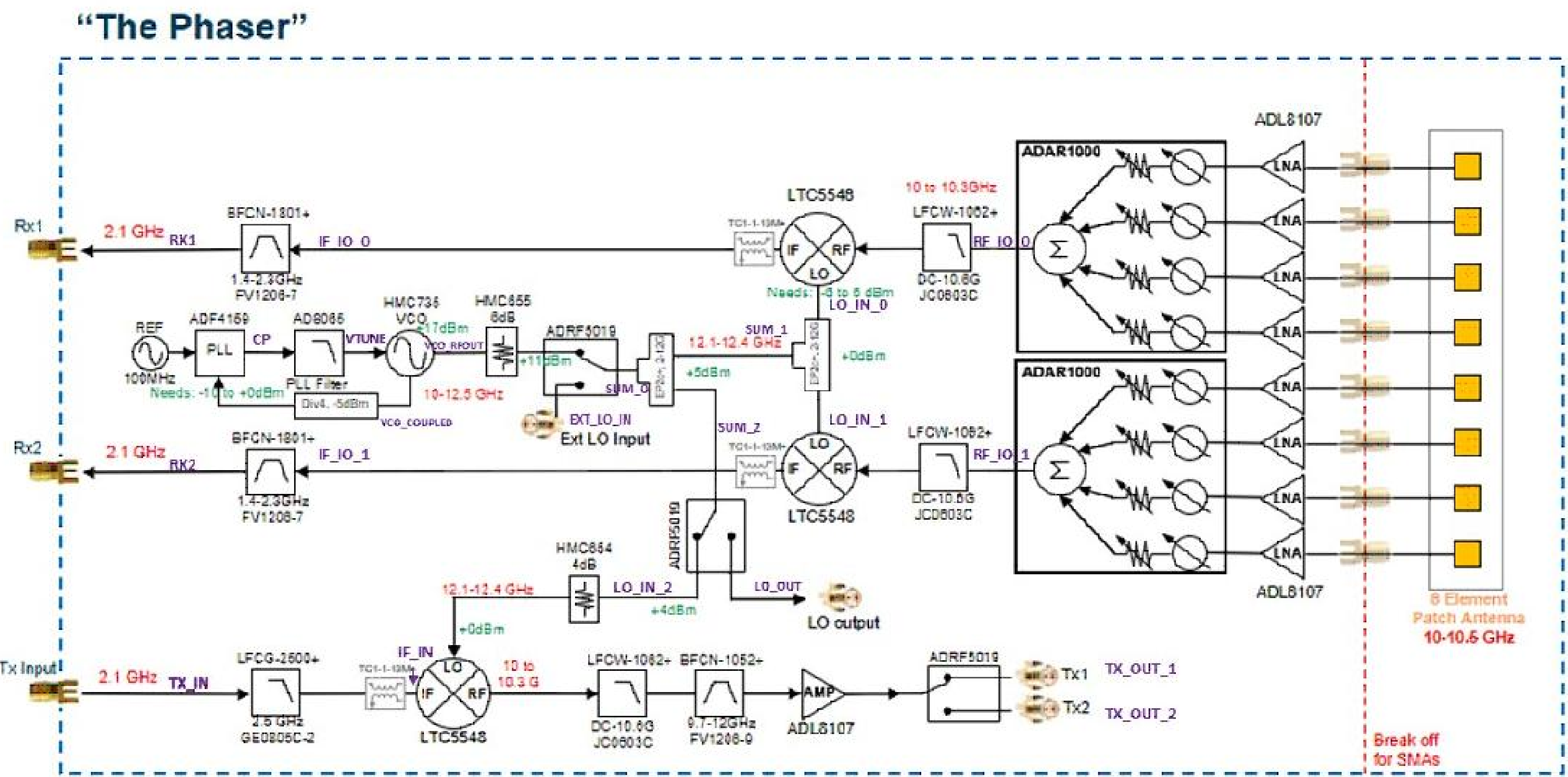


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D	THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED, IN WHOLE OR IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS, OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS OF ANALOG DEVICES. THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY ANALOG DEVICES.					<div>JUMPER TABLE</div> <table><tr><td>JP#</td><td>ON</td><td>OFF</td></tr><tr><td>1</td><td></td><td></td></tr><tr><td>2</td><td></td><td></td></tr><tr><td>3</td><td></td><td></td></tr><tr><td>4</td><td></td><td></td></tr><tr><td>5</td><td></td><td></td></tr></table> <div>* SEE ASSEMBLY INSTRUCTIONS</div>					JP#	ON	OFF	1			2			3			4			5			<div>REVISIONS</div> <table><tr><td>REV</td><td>DESCRIPTION</td><td>DATE</td><td>APPROVED</td></tr><tr><td>A</td><td>INITIAL RELEASE</td><td>03NOV21</td><td>T.CABILDO</td></tr><tr><td>B</td><td>CHANGES AS PER ECR-107288</td><td>11MAY22</td><td>T.CABILDO</td></tr><tr><td>B1</td><td>CHANGES AS PER ECR-112257</td><td>28DEC22</td><td>T.CABILDO</td></tr><tr><td>C</td><td>CHANGES AS PER ECR-113923</td><td>26APR23</td><td>T.CABILDO</td></tr></table>					REV	DESCRIPTION	DATE	APPROVED	A	INITIAL RELEASE	03NOV21	T.CABILDO	B	CHANGES AS PER ECR-107288	11MAY22	T.CABILDO	B1	CHANGES AS PER ECR-112257	28DEC22	T.CABILDO	C	CHANGES AS PER ECR-113923	26APR23	T.CABILDO
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CONTROL	CODE	DEVICE	FUNCTION	CONNECTOR																																																	
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<table><tr><td>TEMPLATE ENGINEER -</td><td>DATE</td><td colspan="3" rowspan="2">SCHEMATIC</td><td colspan="2" rowspan="2"></td></tr><tr><td>HARDWARE SERVICES M.VALE</td><td>03NOV21</td></tr><tr><td>HARDWARE SYSTEMS -</td><td></td><td colspan="5" rowspan="5">HW TYPE : Customer Evaluation z Product(s): ADAR1000 <PRODUCT_1> <DRAWING_TITLE1> <DRAWING_TITLE2> <DRAWING_TITLE3> <DRAWING_TITLE4> <DRAWING_TITLE5></td></tr><tr><td>TEST ENGINEER -</td><td></td></tr><tr><td>COMPONENT ENGINEER M.YAN</td><td>03NOV21</td></tr><tr><td>TEST PROCESS -</td><td></td></tr><tr><td>HARDWARE RELEASE K.JABATAN</td><td>03NOV21</td></tr><tr><td>DESIGNER G.GARCIA</td><td>03NOV21</td><td>MASTER PROJECT TEMPLATE <DRAWING_TITLE6></td><td>TESTER TEMPLATE no_template</td><td colspan="2" rowspan="2">DRAWING NO. 02_066247</td><td rowspan="2">REV. C</td></tr><tr><td>PTD ENGINEER T.CABILDO</td><td>03NOV21</td><td colspan="2">UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES</td></tr><tr><td>CHECKER -</td><td></td><td colspan="2">DECIMALS X.XX +0.010 X.XXX +0.005</td><td>FRACTIONS +-1/32</td><td>ANGLES +-2</td><td>SIZE D</td><td>SCALE <SCALE>-</td><td>CODE ID NO.</td><td>SHEET 1</td><td>OF 12</td></tr></table>					TEMPLATE ENGINEER -	DATE	SCHEMATIC					HARDWARE SERVICES M.VALE	03NOV21	HARDWARE SYSTEMS -		HW TYPE : Customer Evaluation z Product(s): ADAR1000 <PRODUCT_1> <DRAWING_TITLE1> <DRAWING_TITLE2> <DRAWING_TITLE3> <DRAWING_TITLE4> <DRAWING_TITLE5>					TEST ENGINEER -		COMPONENT ENGINEER M.YAN	03NOV21	TEST PROCESS -		HARDWARE RELEASE K.JABATAN	03NOV21	DESIGNER G.GARCIA	03NOV21	MASTER PROJECT TEMPLATE <DRAWING_TITLE6>	TESTER TEMPLATE no_template	DRAWING NO. 02_066247		REV. C	PTD ENGINEER T.CABILDO	03NOV21	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES		CHECKER -		DECIMALS X.XX +0.010 X.XXX +0.005		FRACTIONS +-1/32	ANGLES +-2	SIZE D	SCALE <SCALE>-	CODE ID NO.	SHEET 1	OF 12			
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8		7		6		5		4		3		2		1																																							

SYSTEM DIAGRAMS

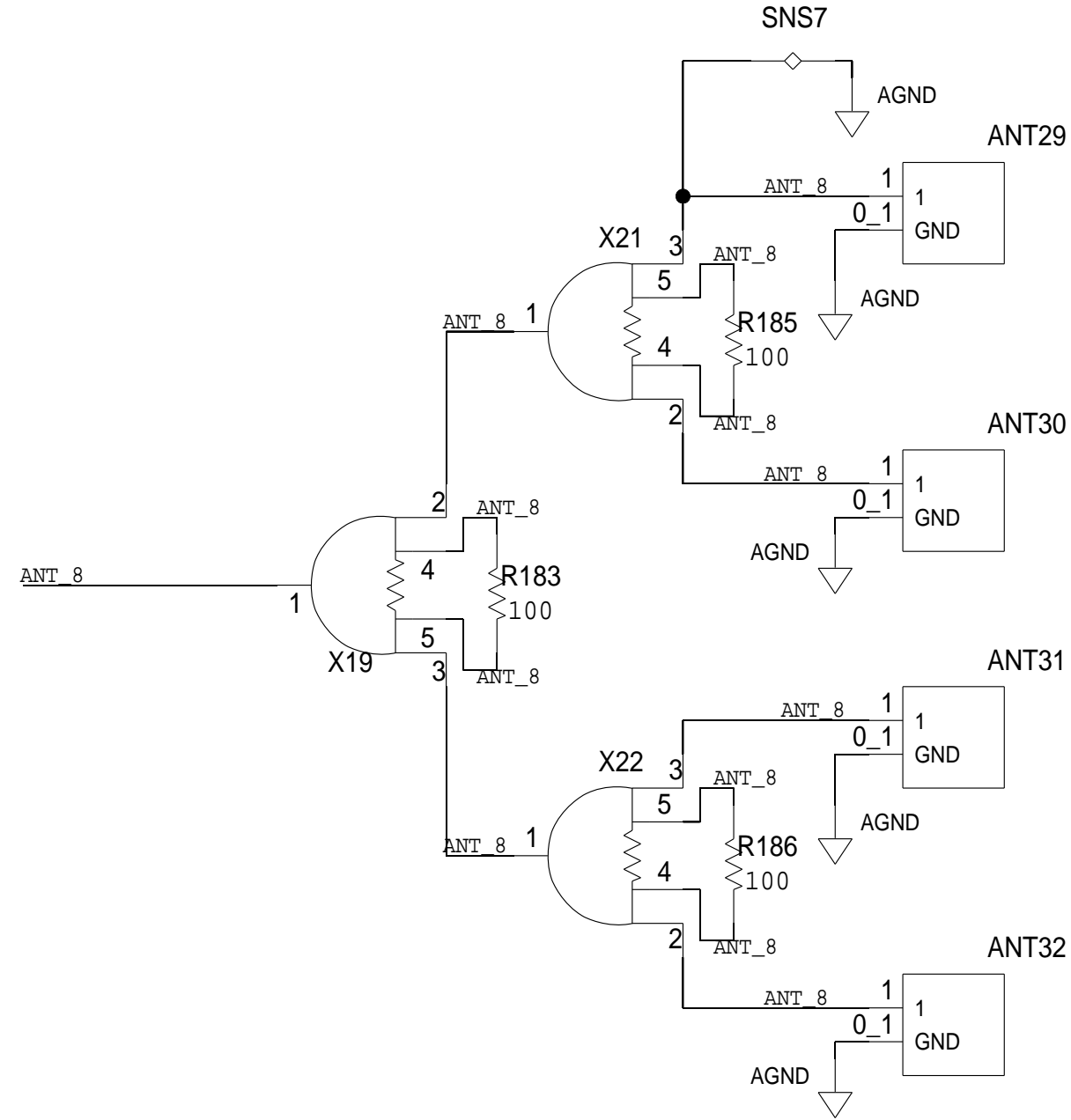
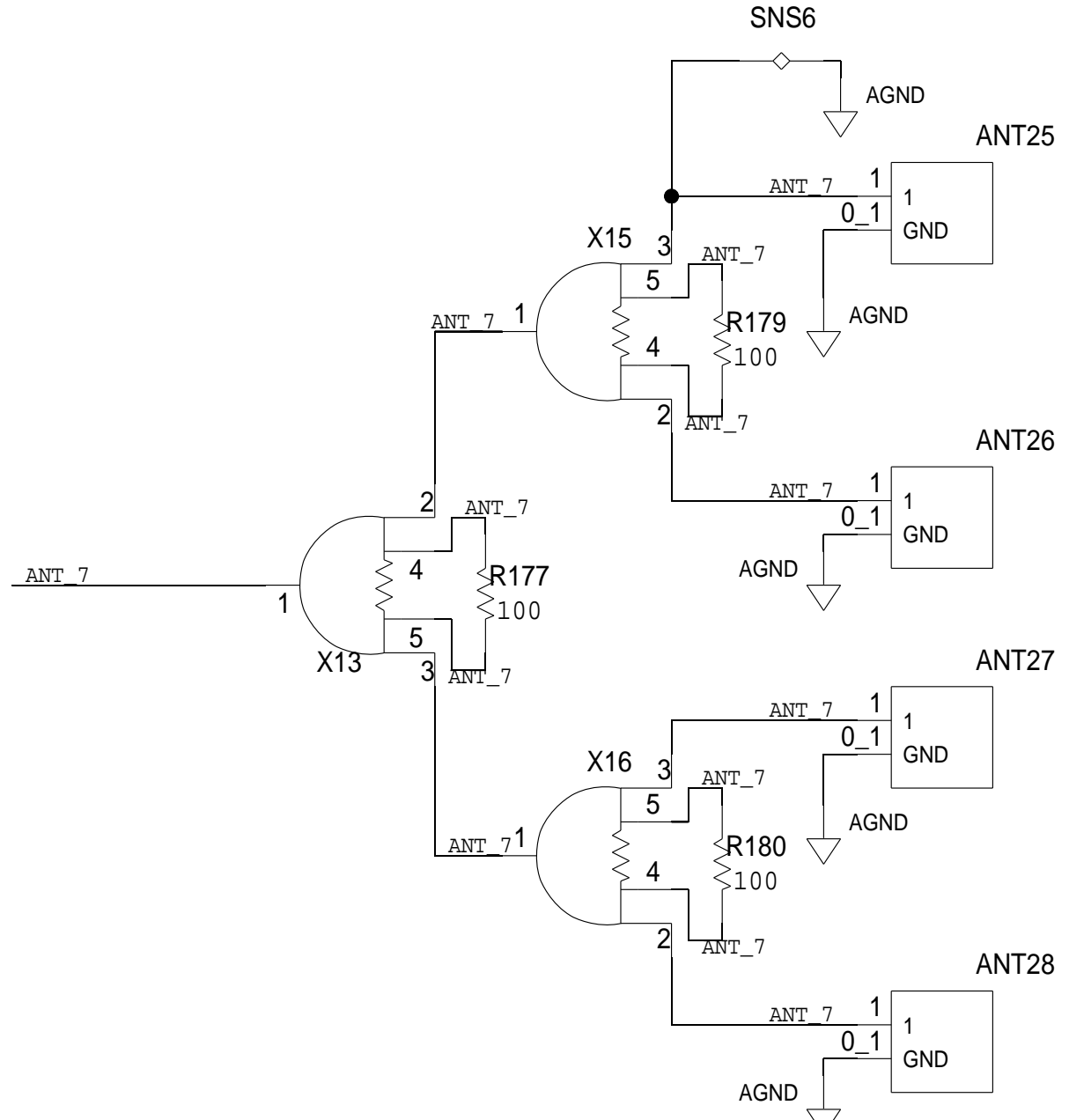
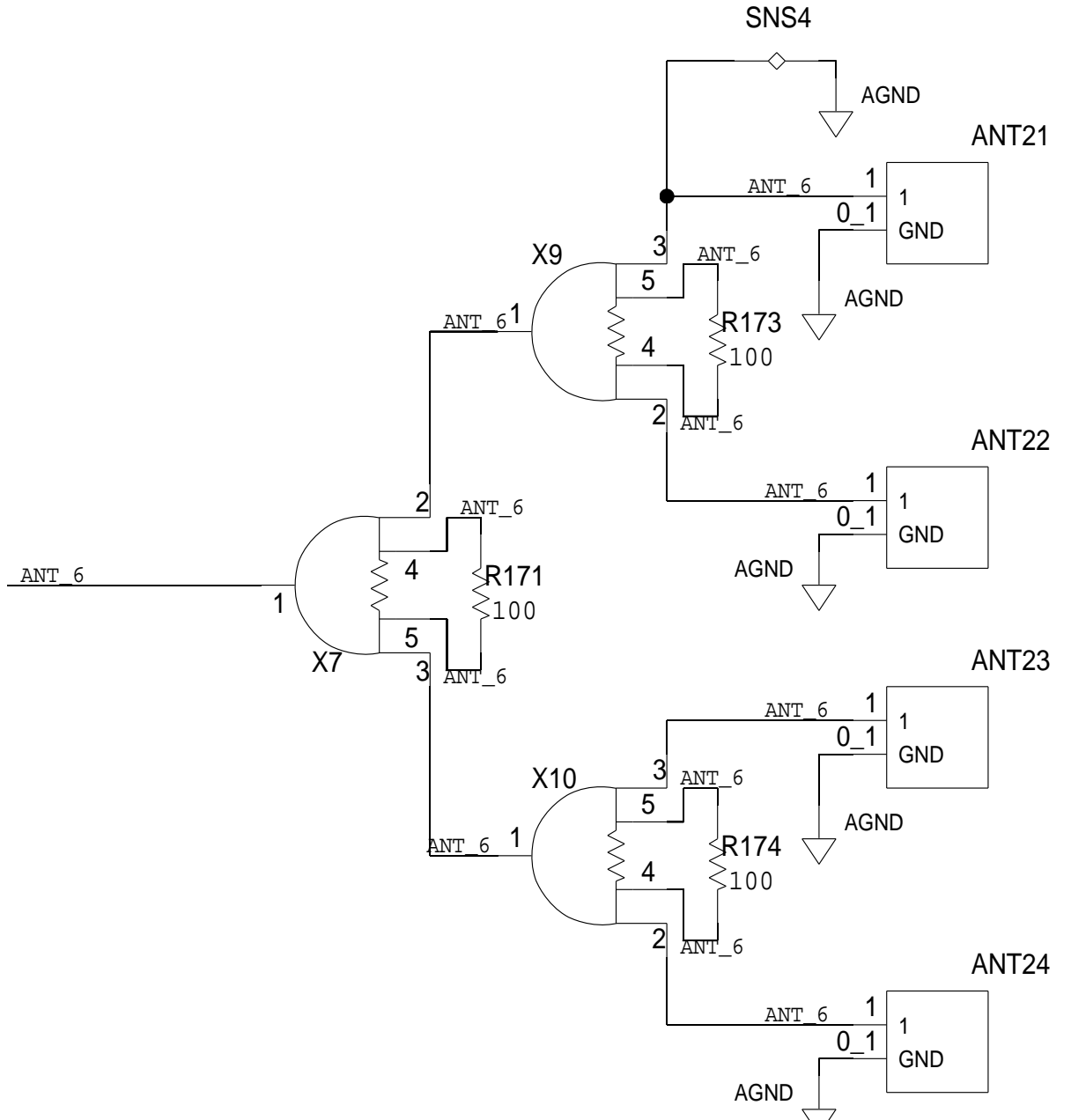
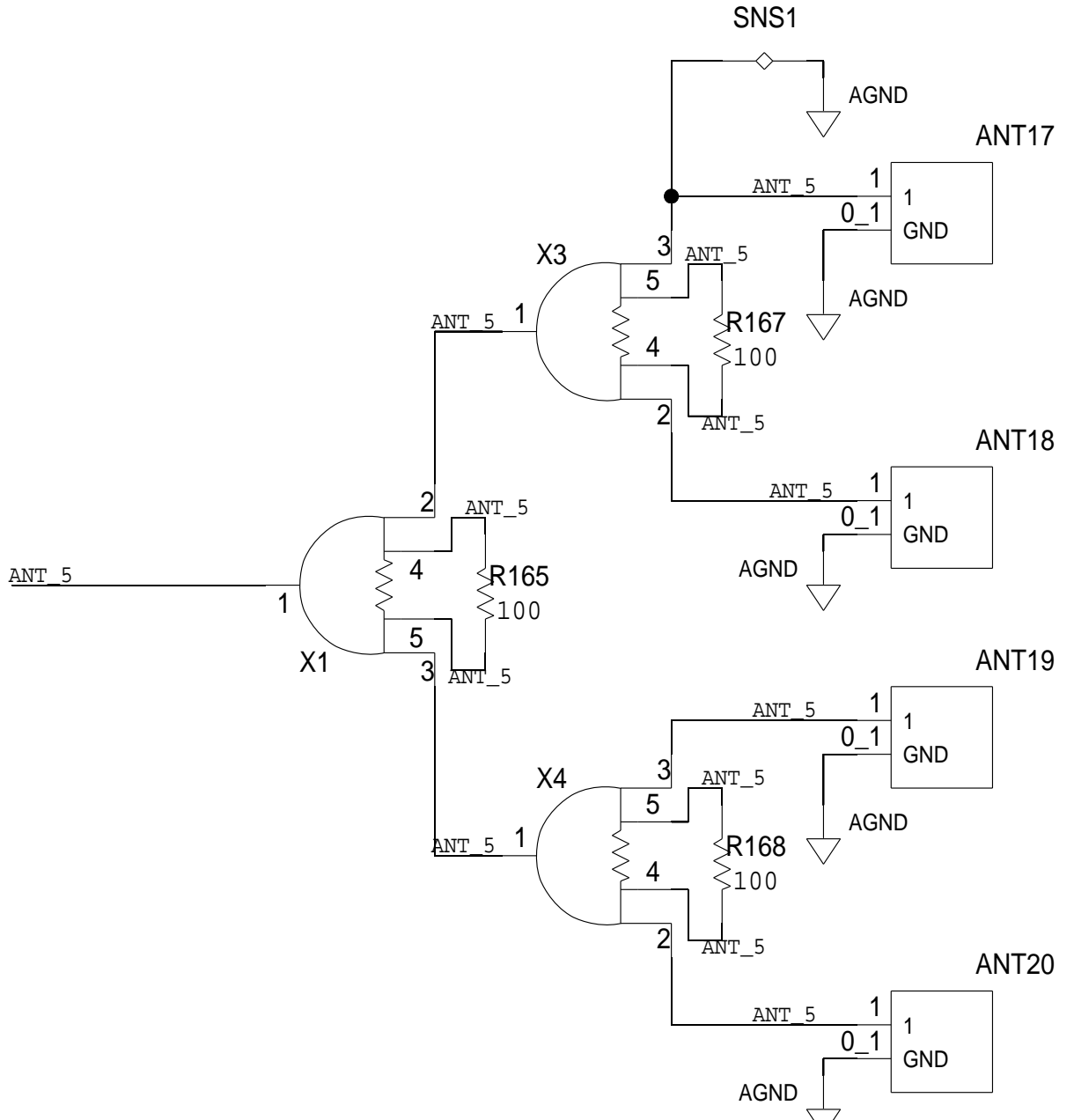
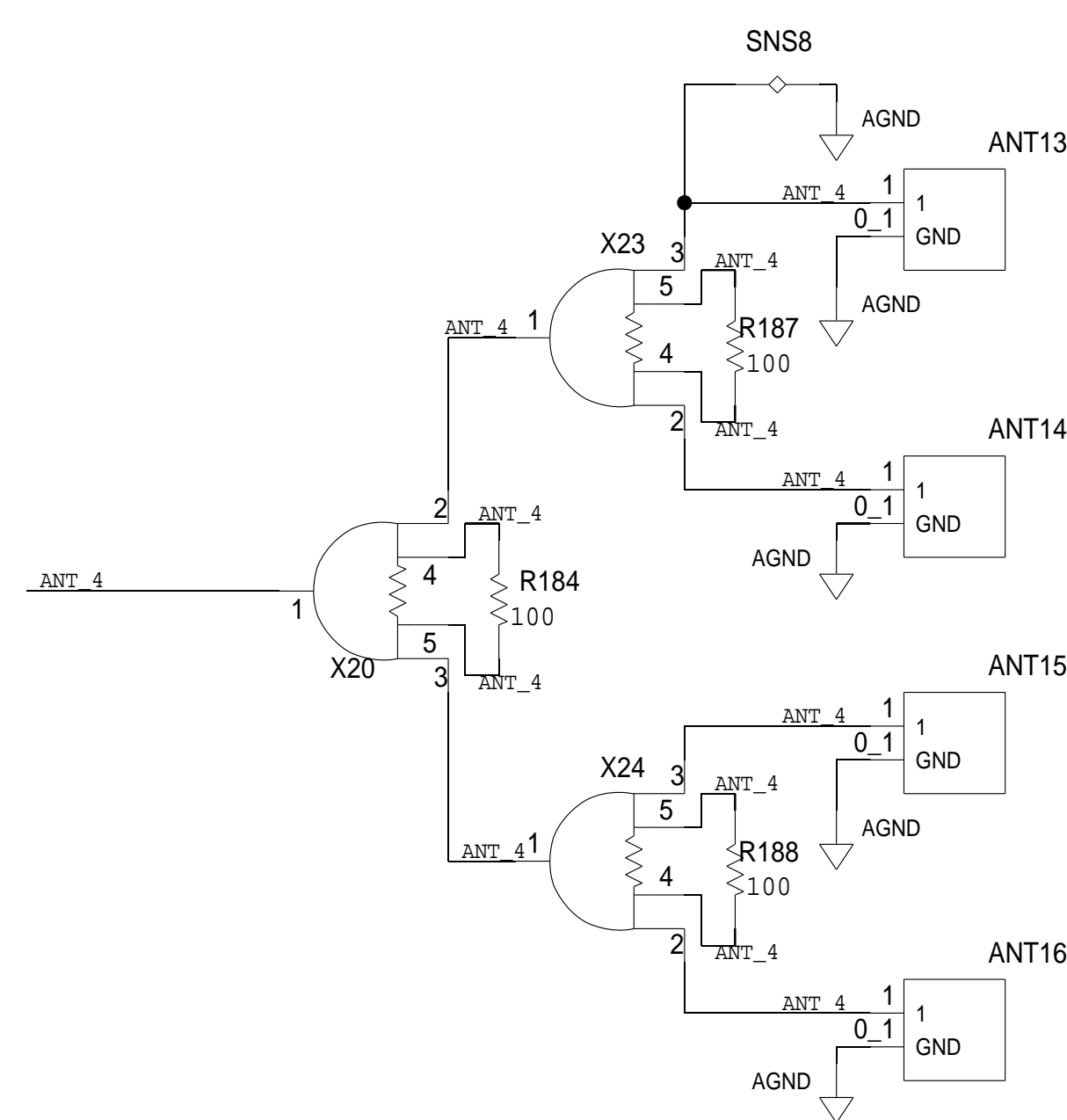
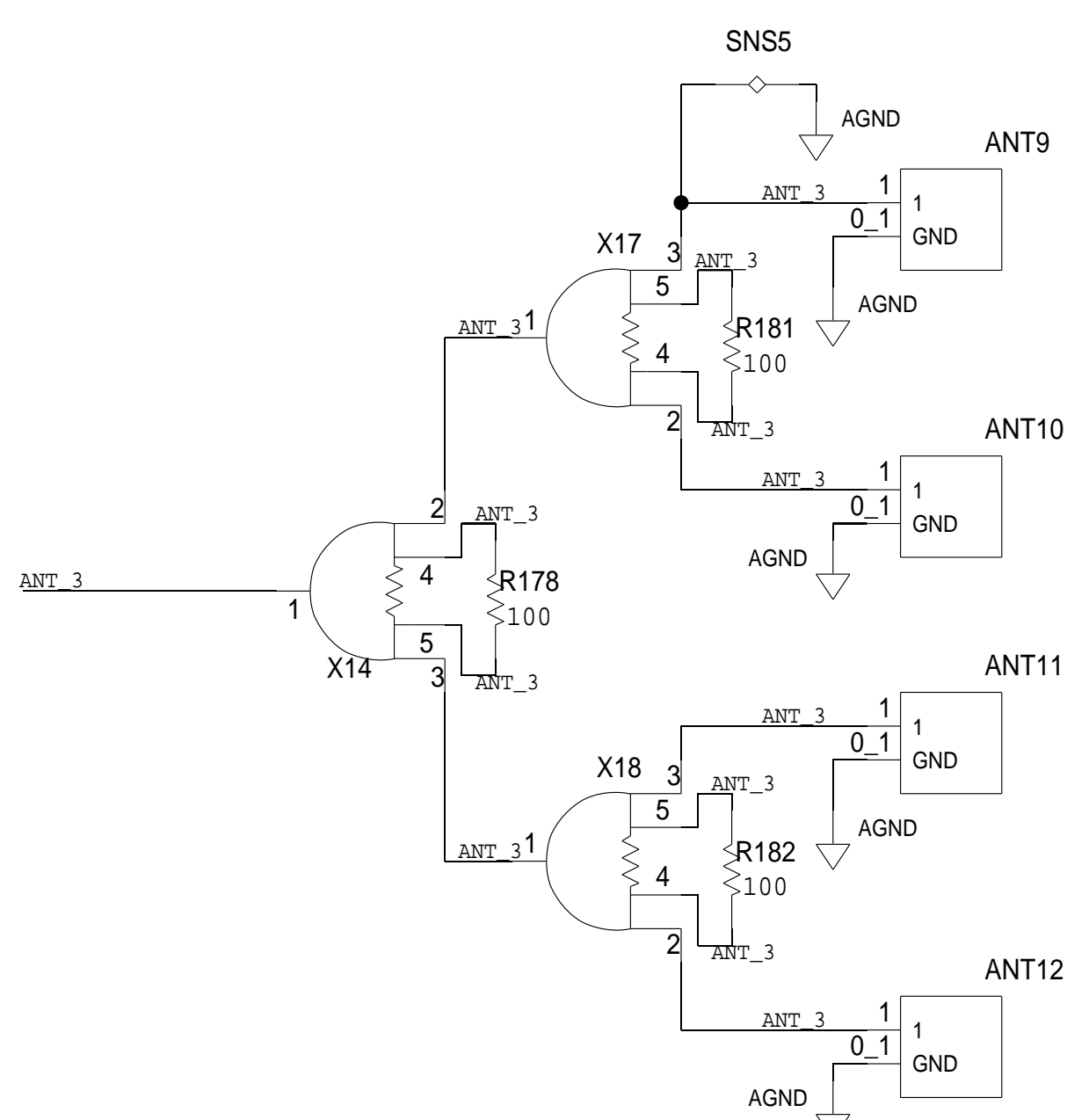
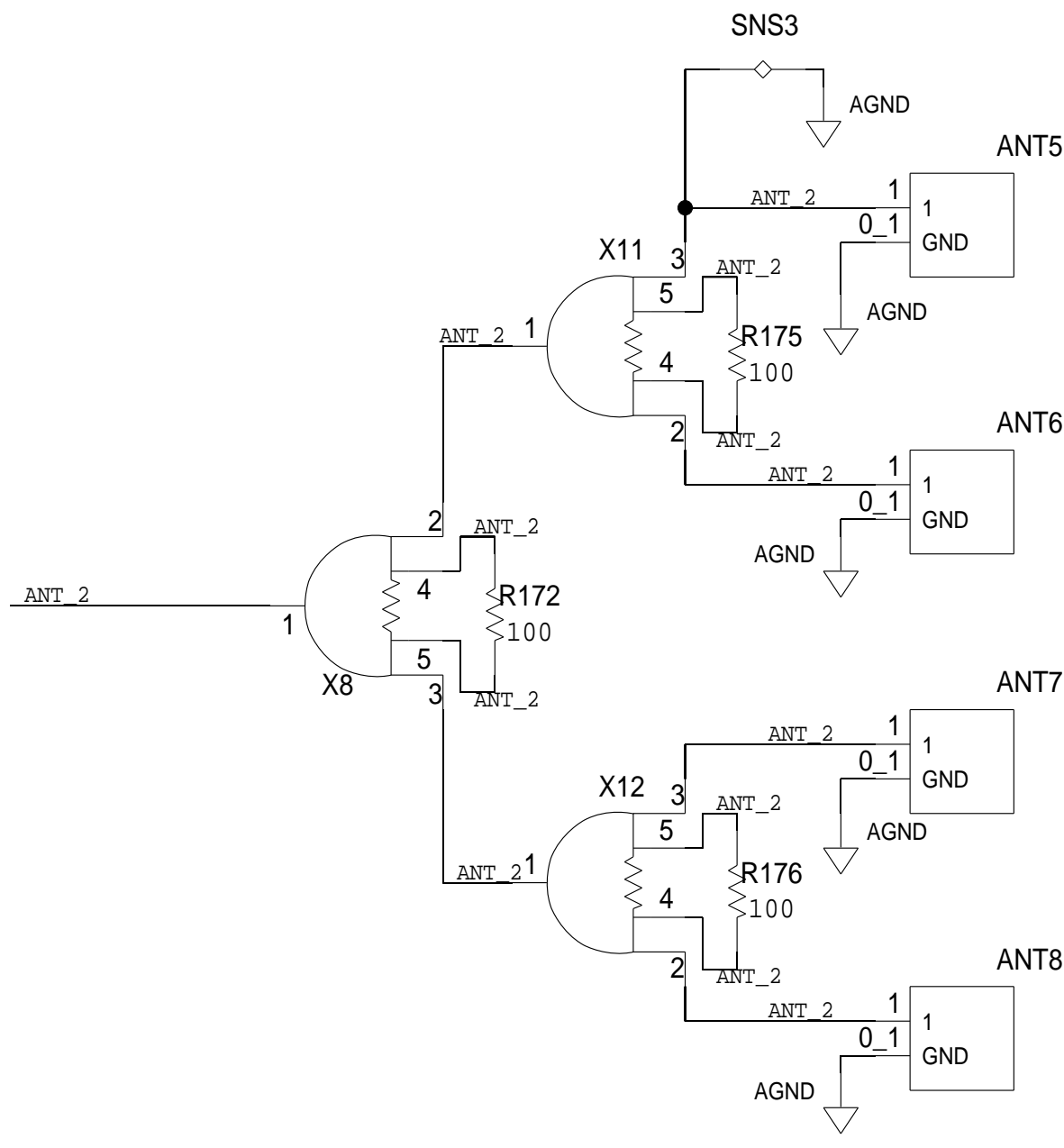
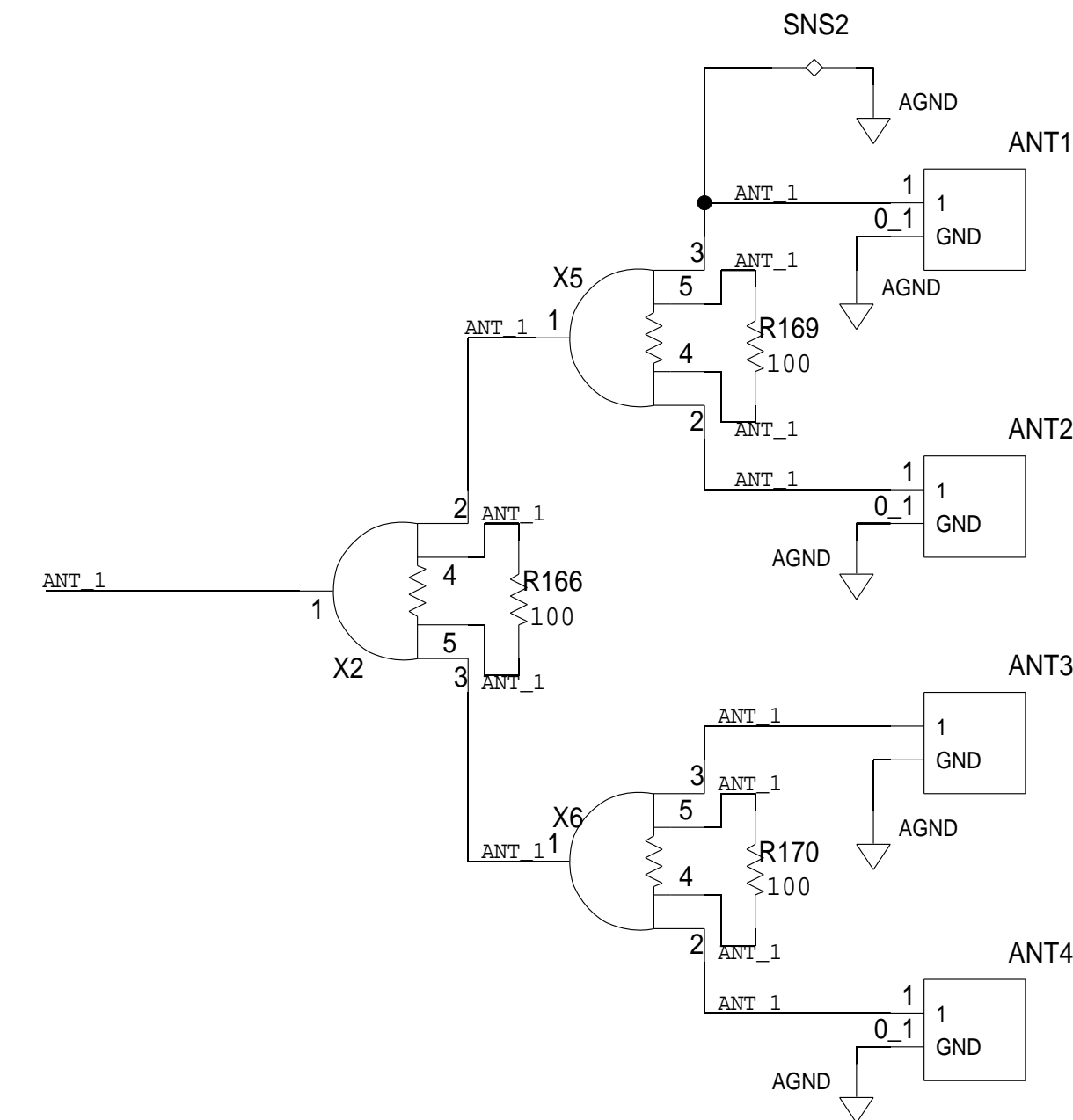
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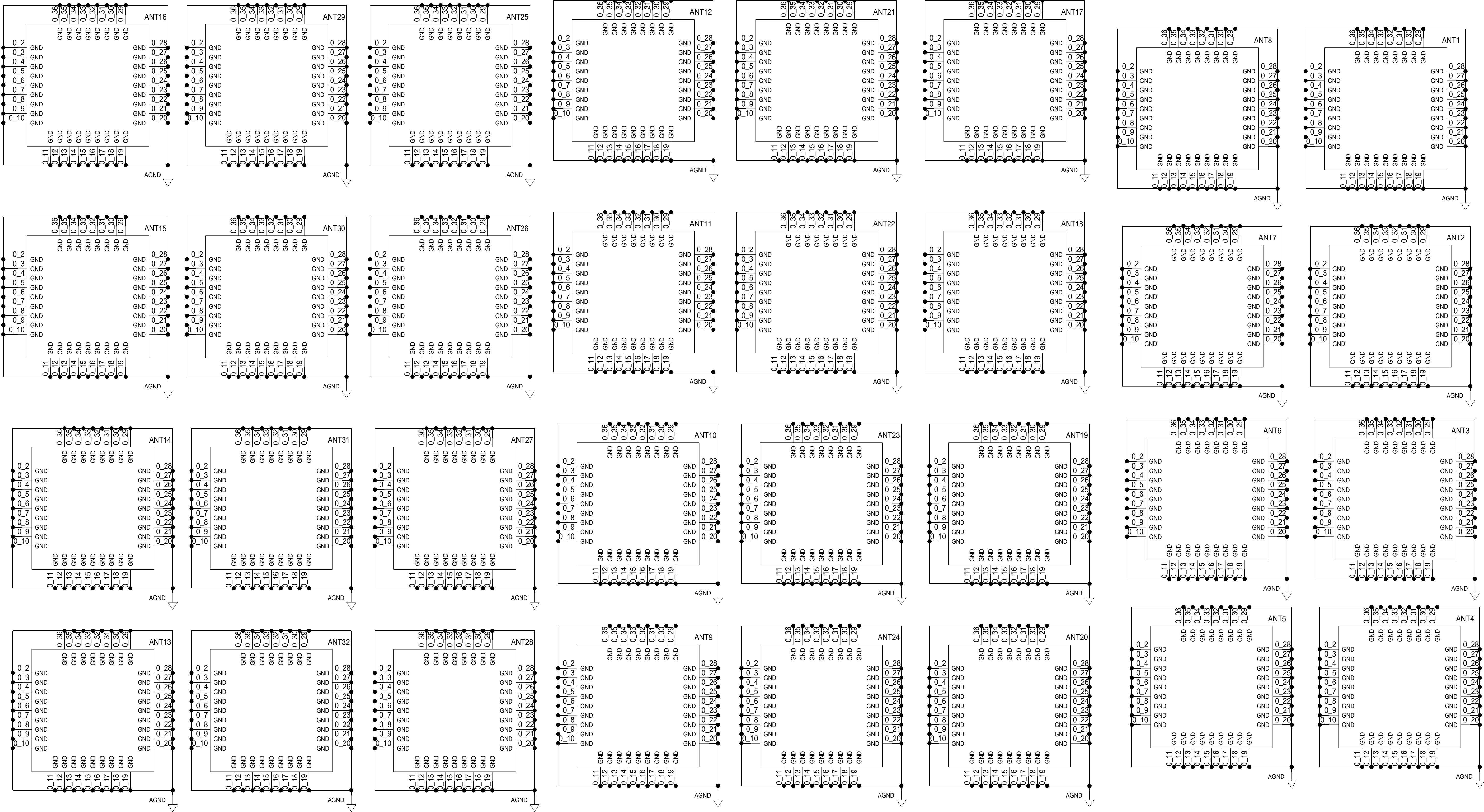
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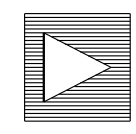


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ANTENNA ARRAY



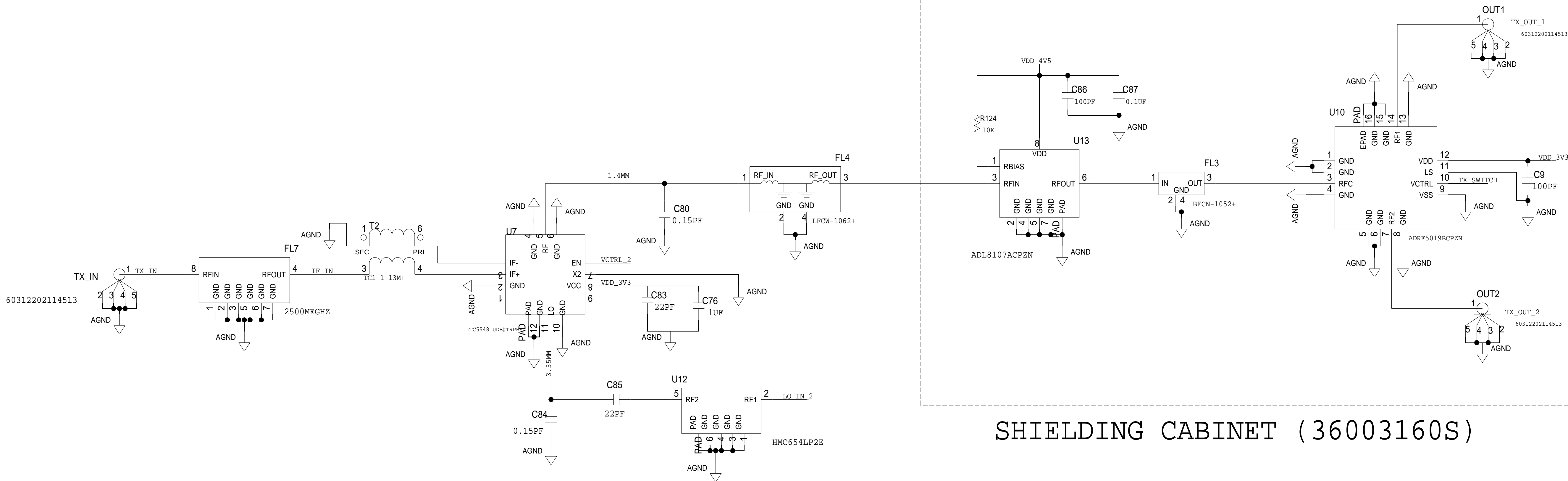
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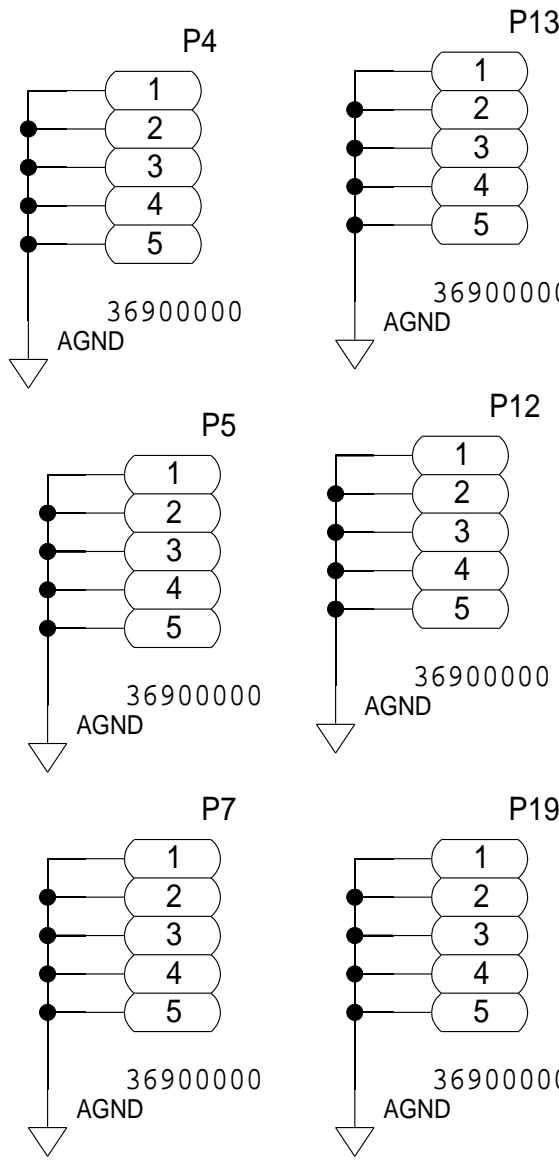
SHEET 4	OF 12
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TX_IN, TX_OUT_1, TX_OUT_2

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



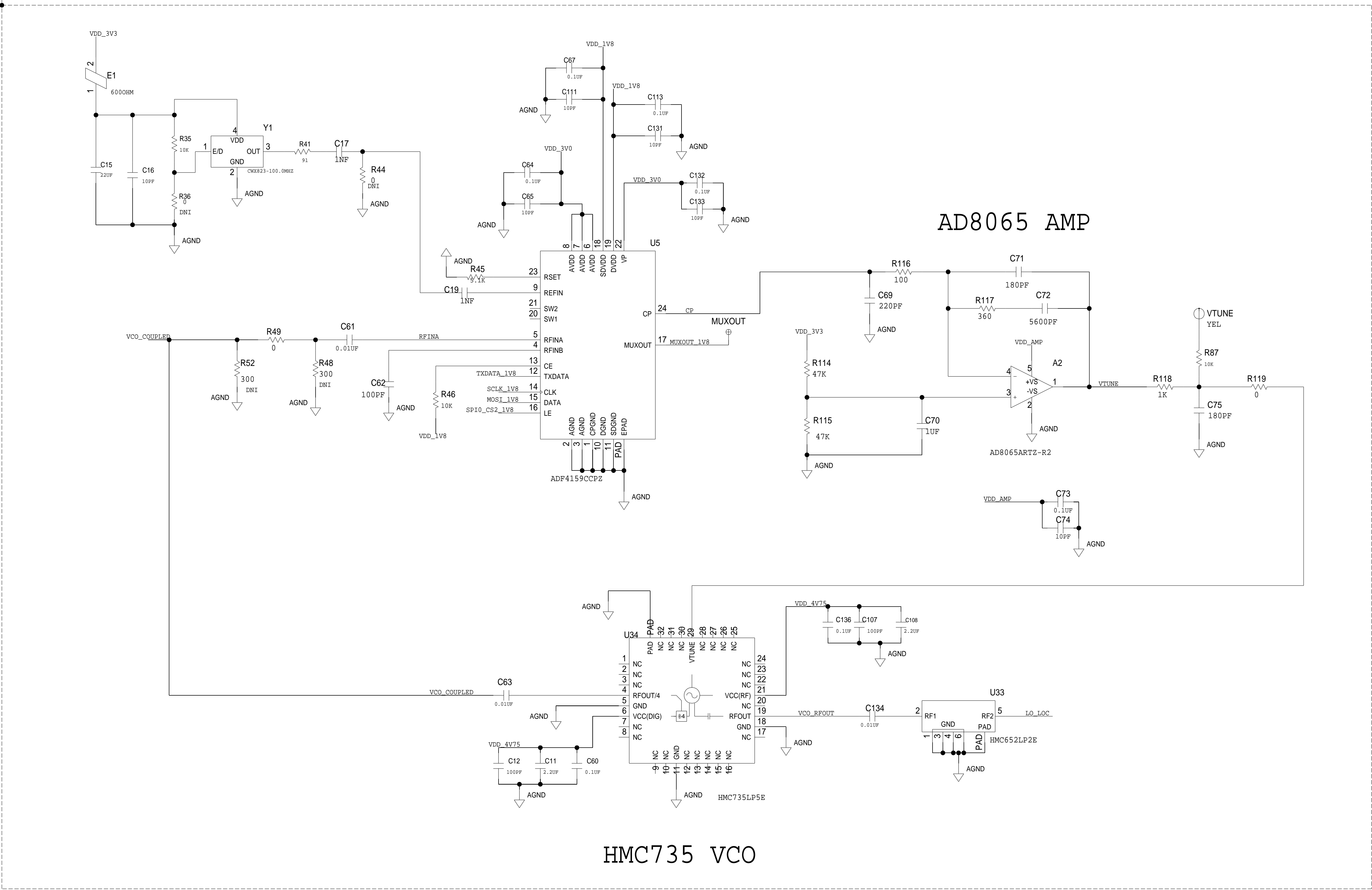
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ADF4159 SYNTHESIZER

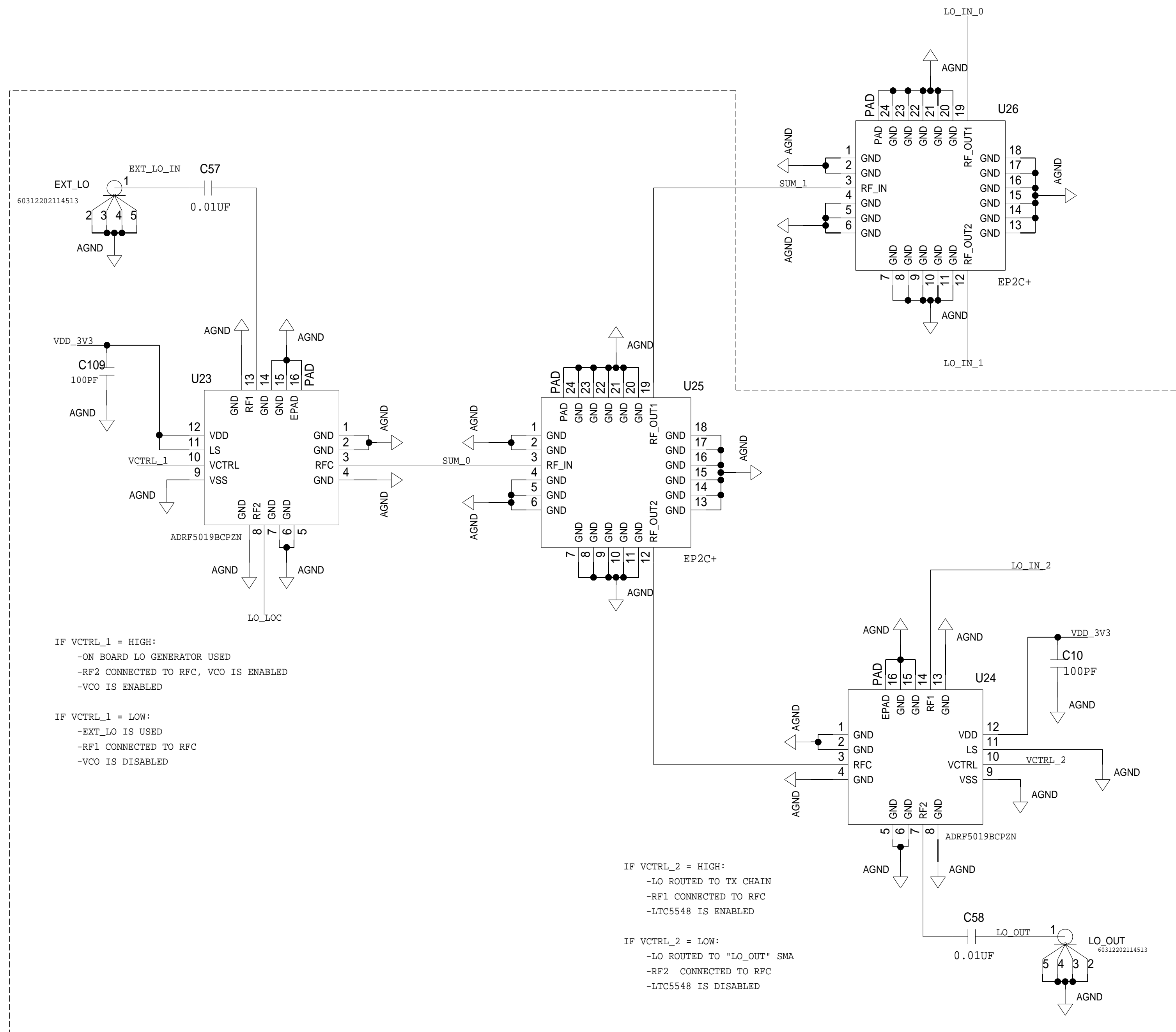


SHIELDING CABINET (36003300S)

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

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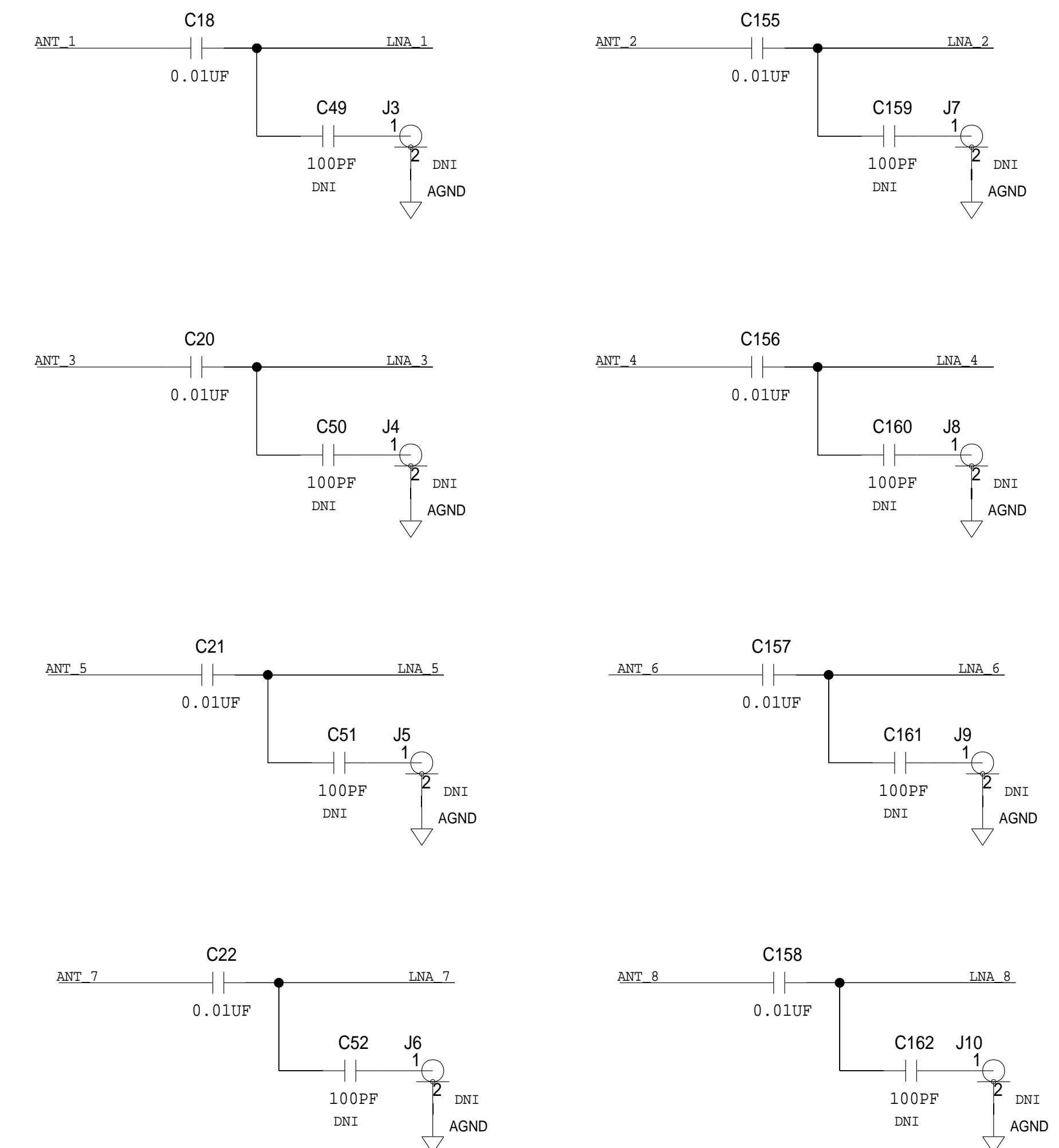
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SHIELDING CABINET (36003300S)

OPTIONAL SMP CONNECTORS

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



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OF ANALOG DEVICES.
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OWNED OR CONTROLLED BY OWNED ANALOG DEVICES.

SCHEMATIC

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Product(s):  ADAR1000
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PTD ENGINEER
T. CABILDO

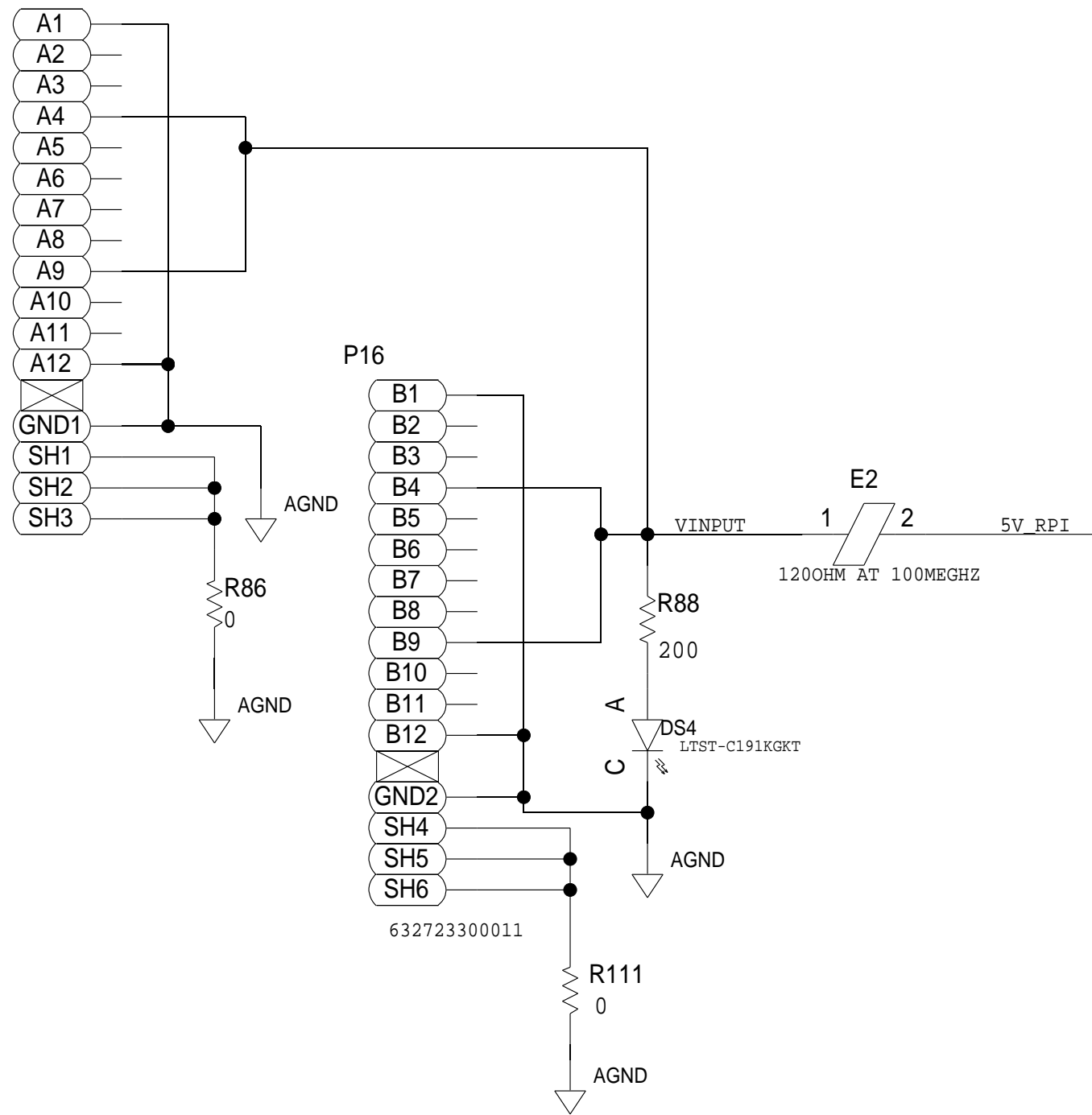
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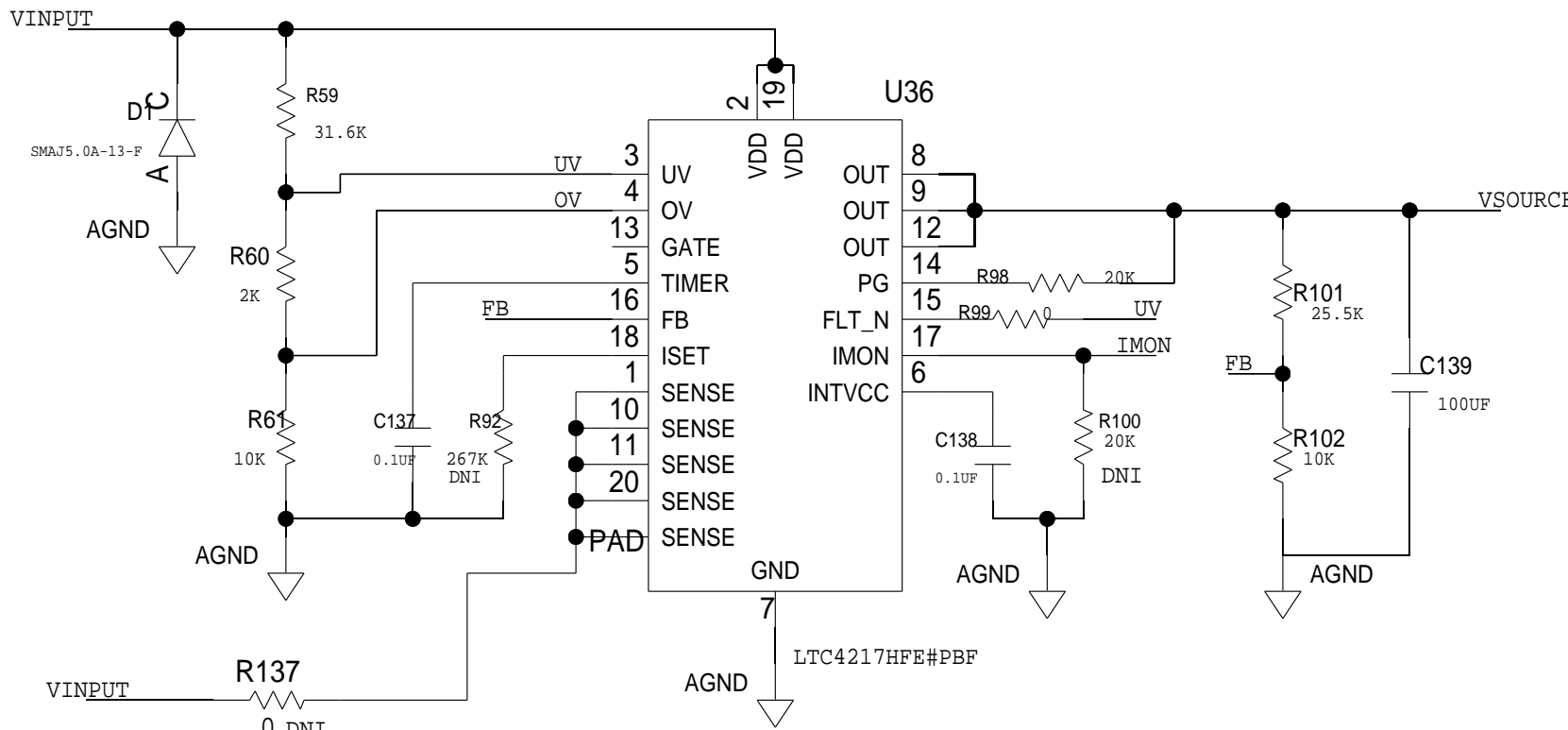
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SHEET 9 OF 12

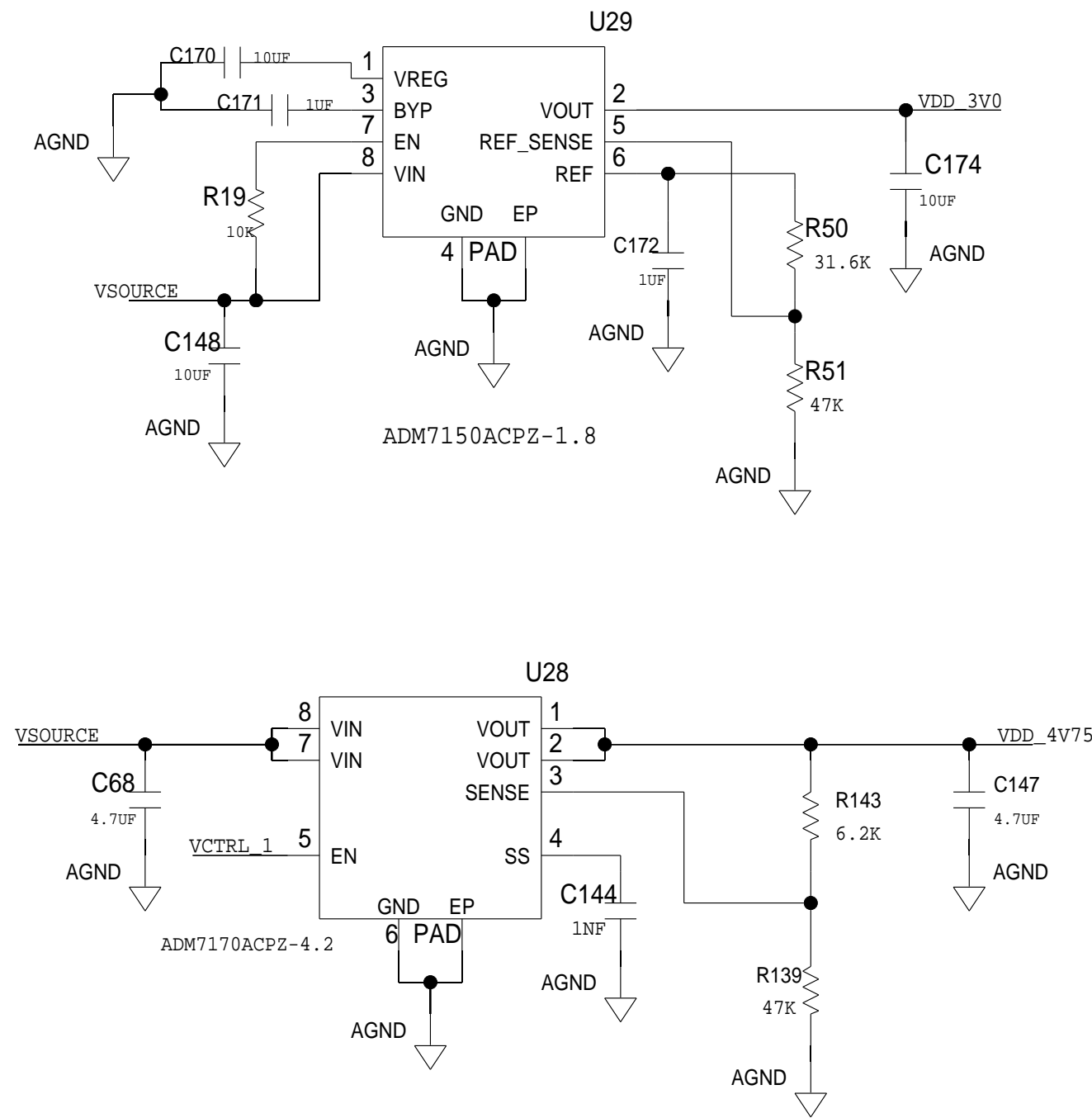
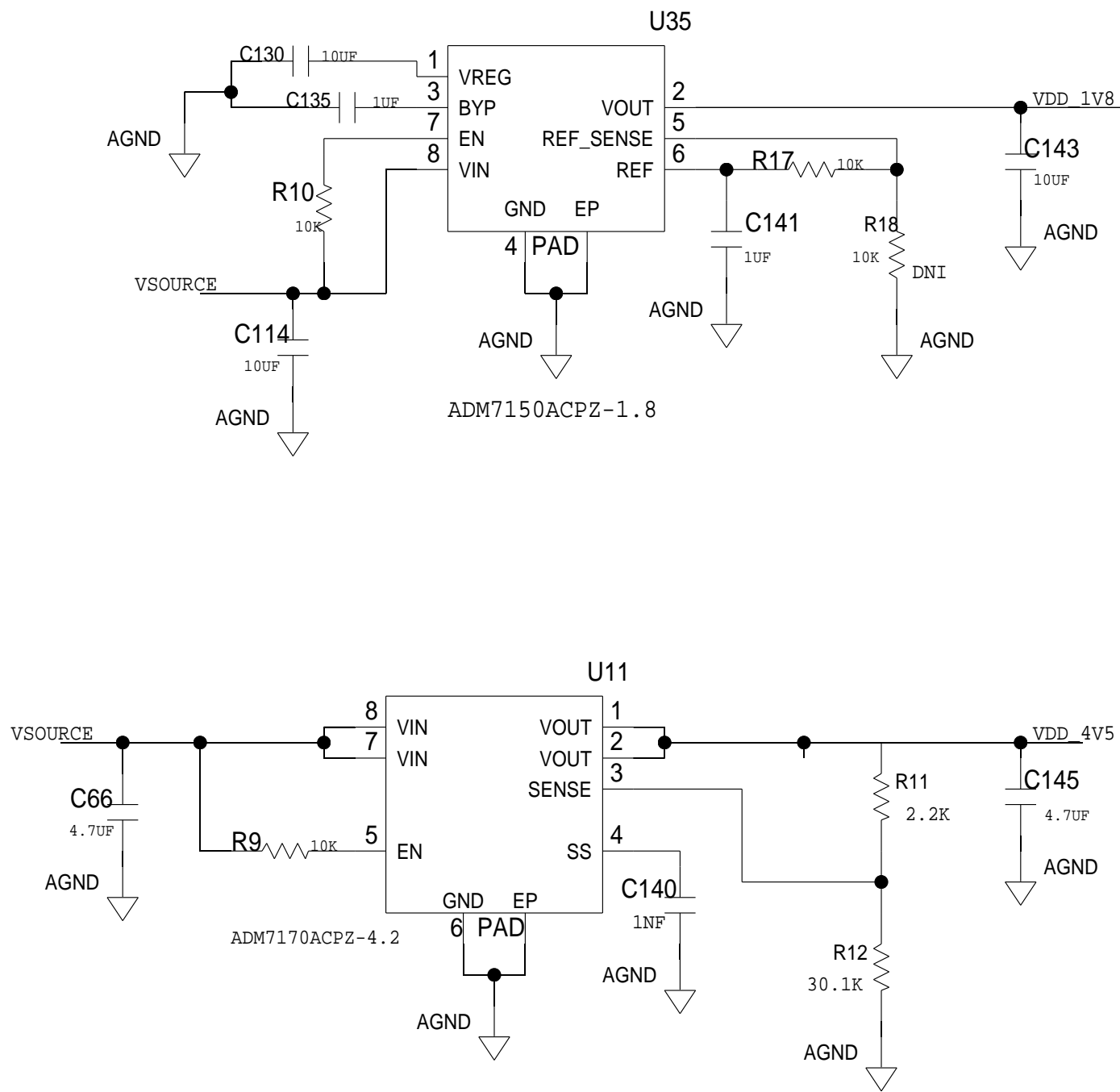
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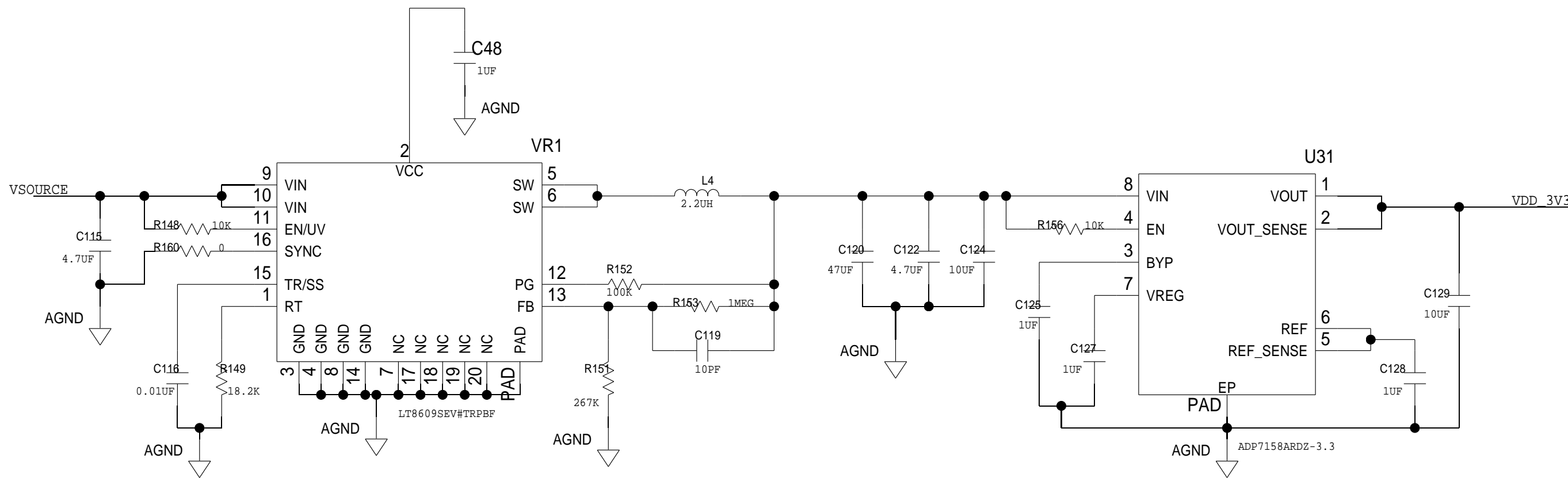
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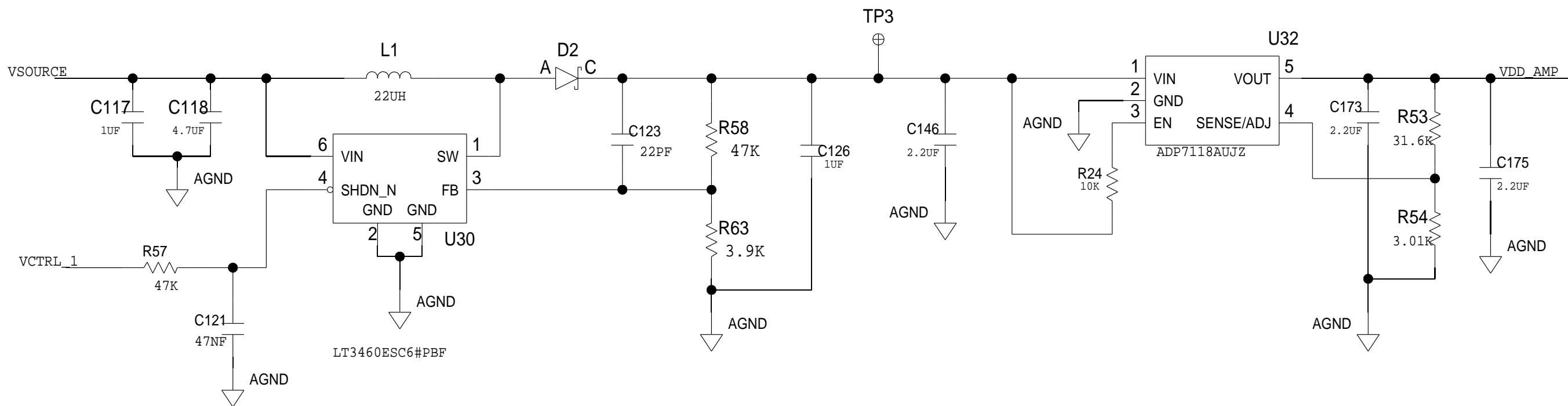
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3.3V SUPPLY



14V SUPPLY

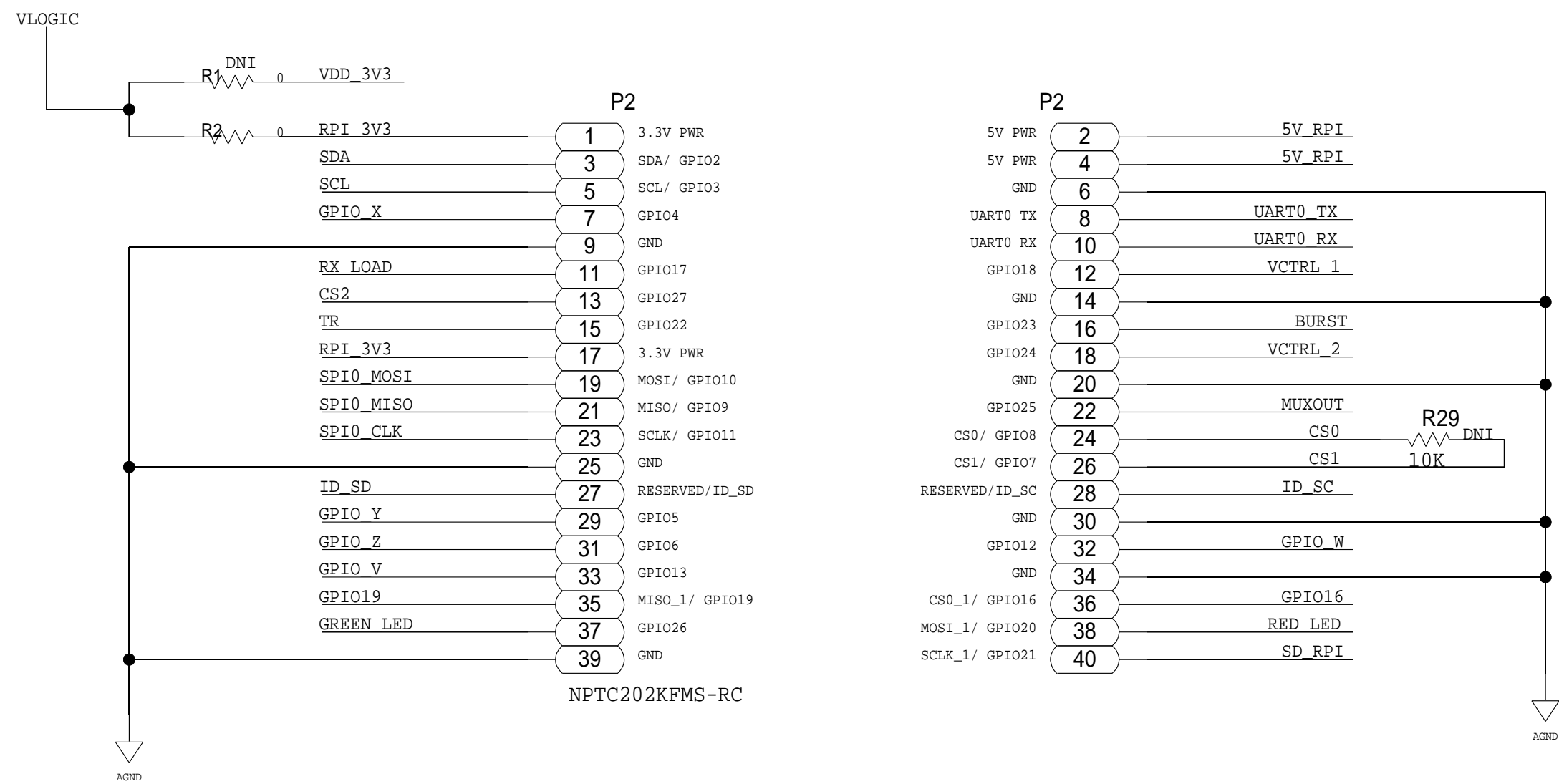


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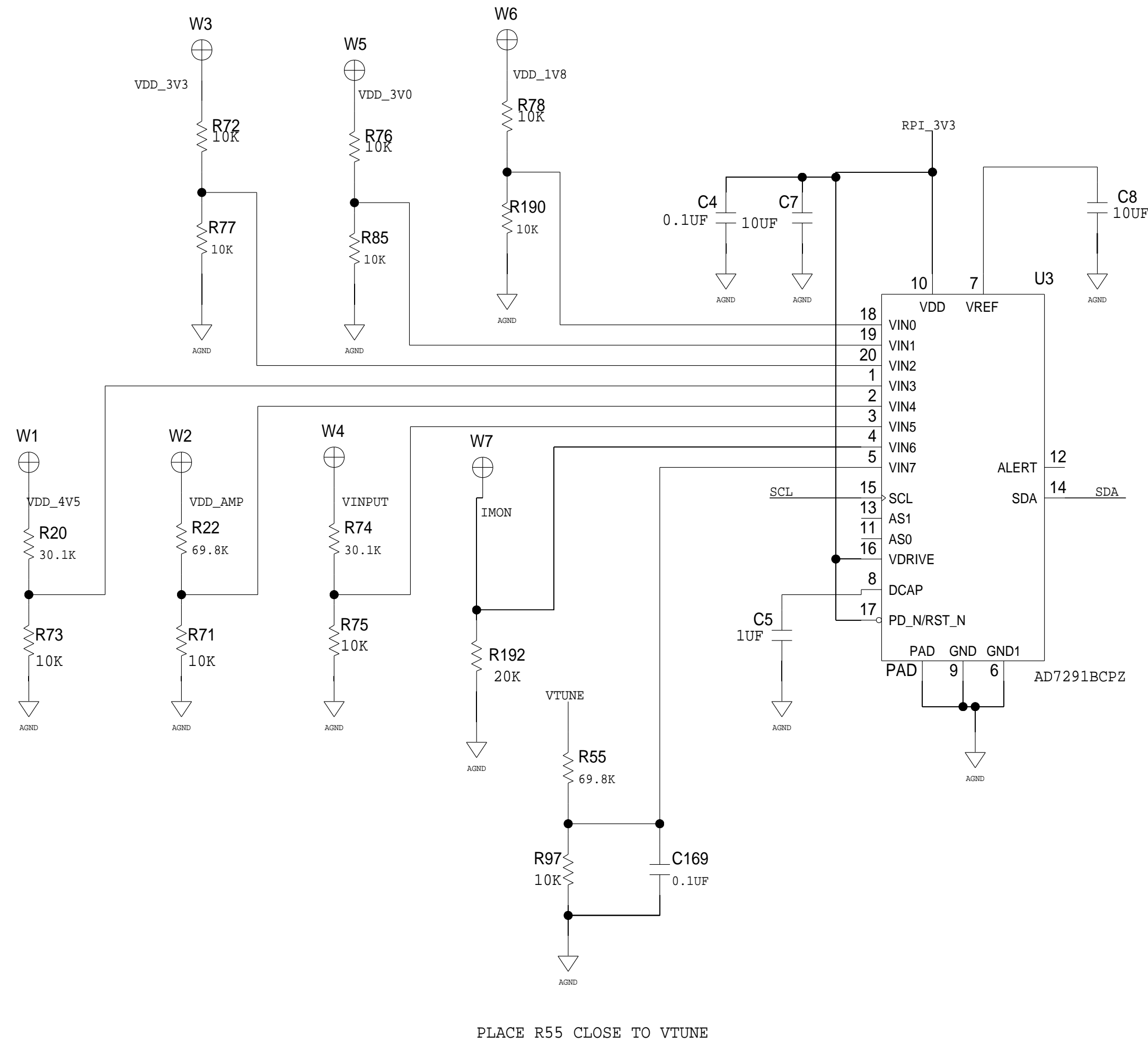
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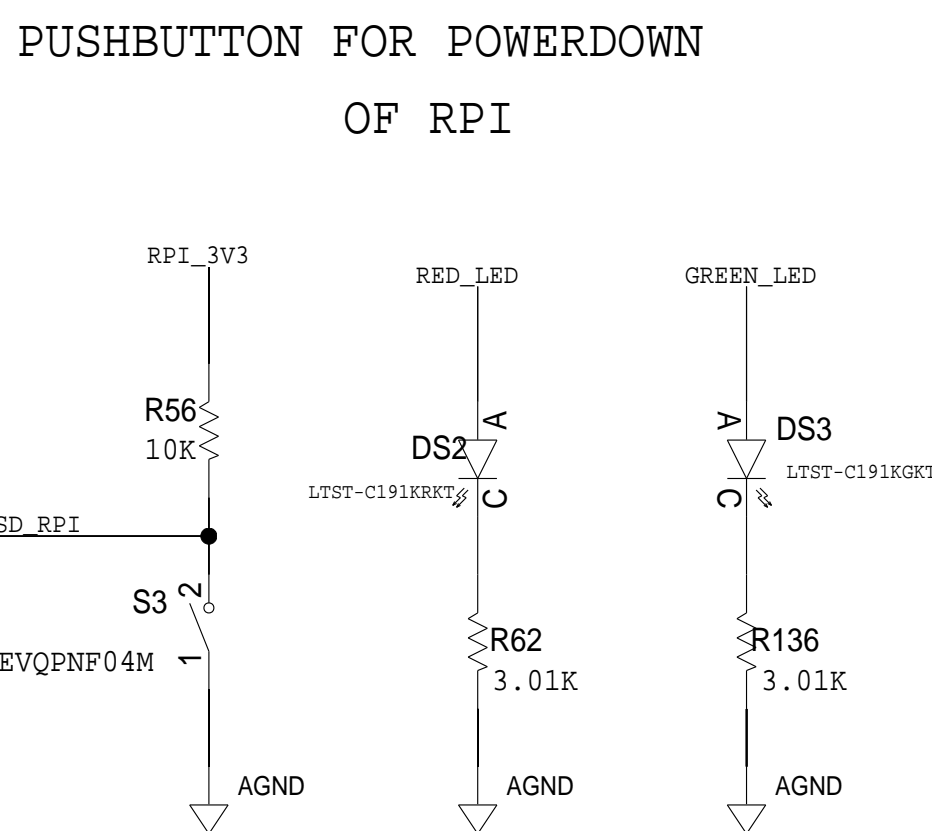
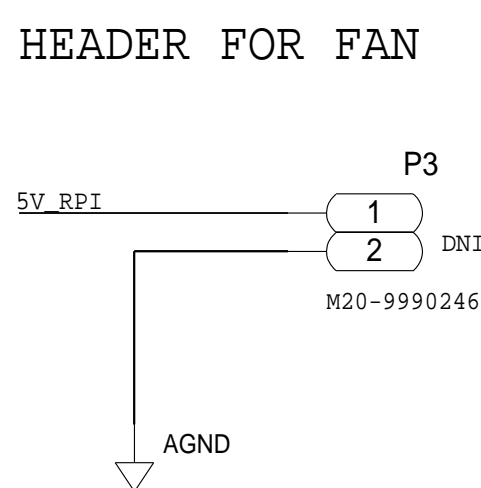
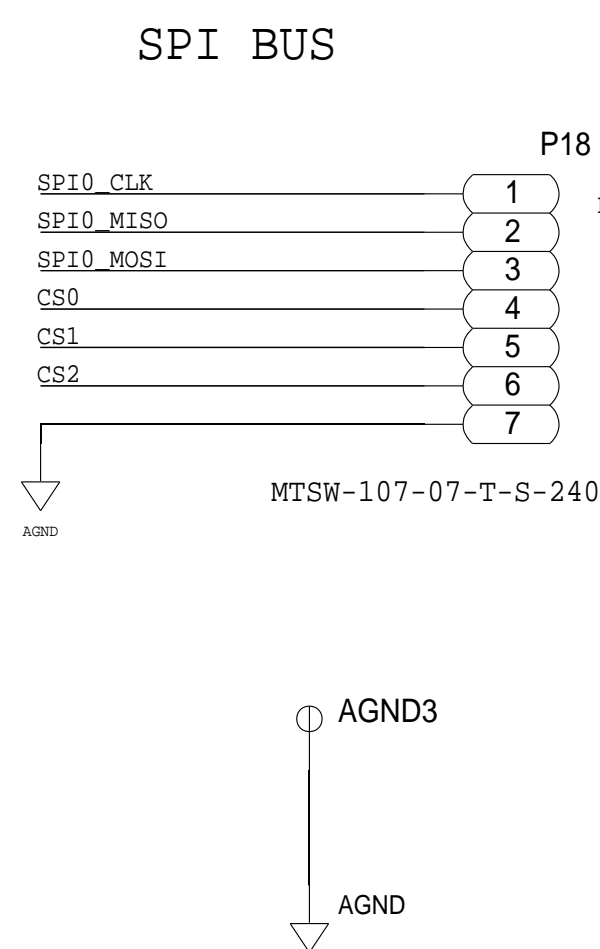
RPI CONNECTIONS



AD7291 ADC



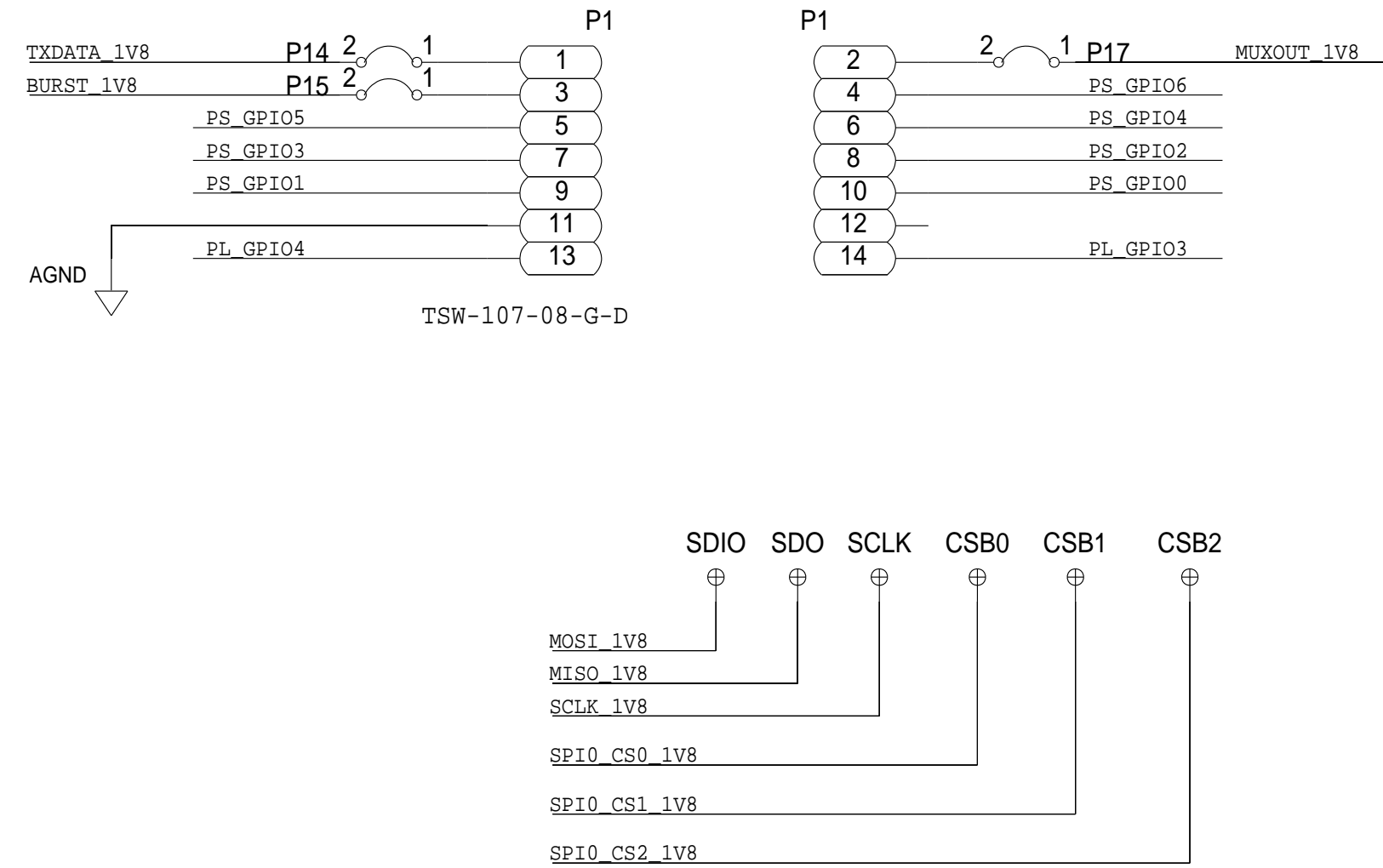
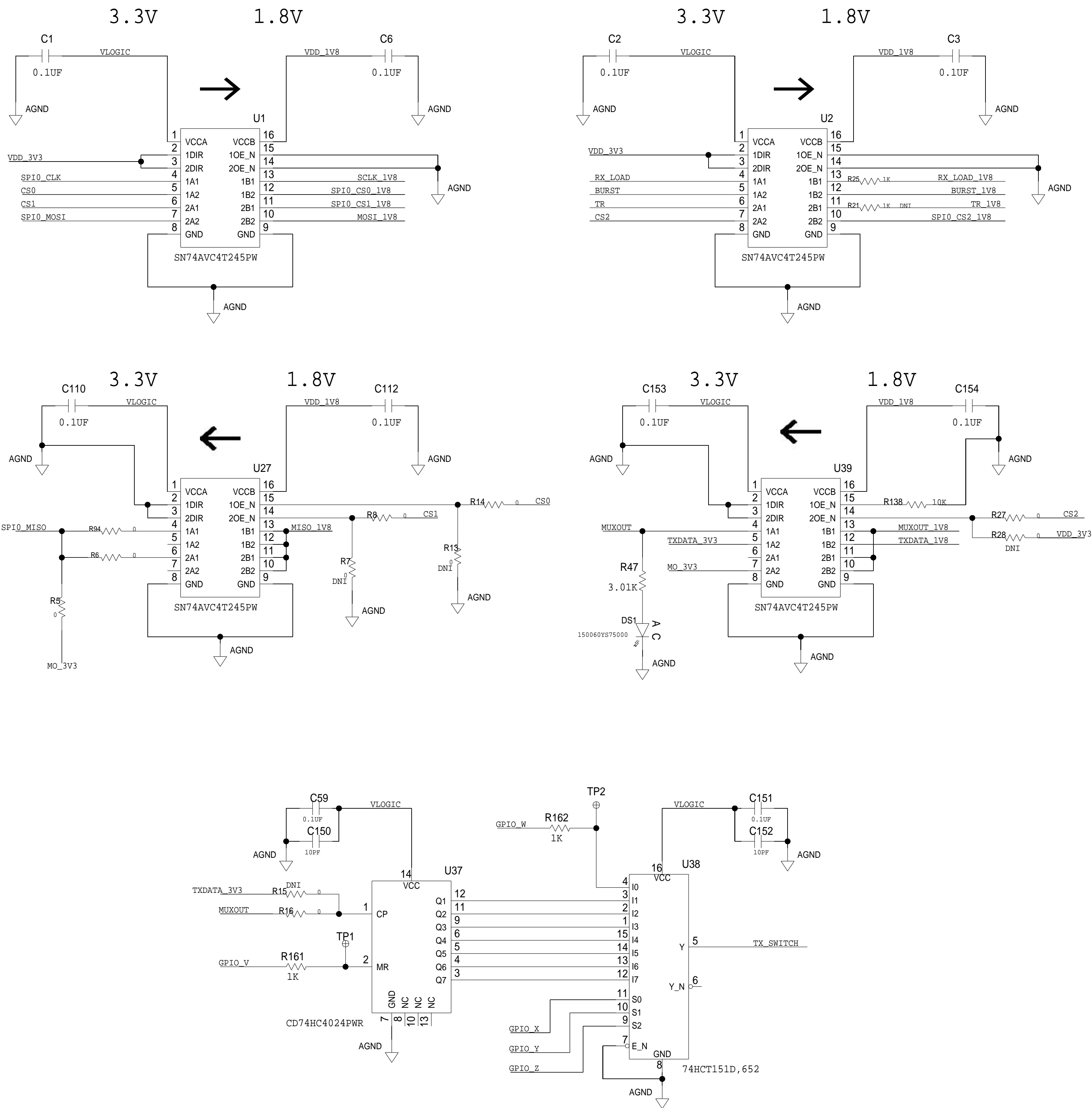
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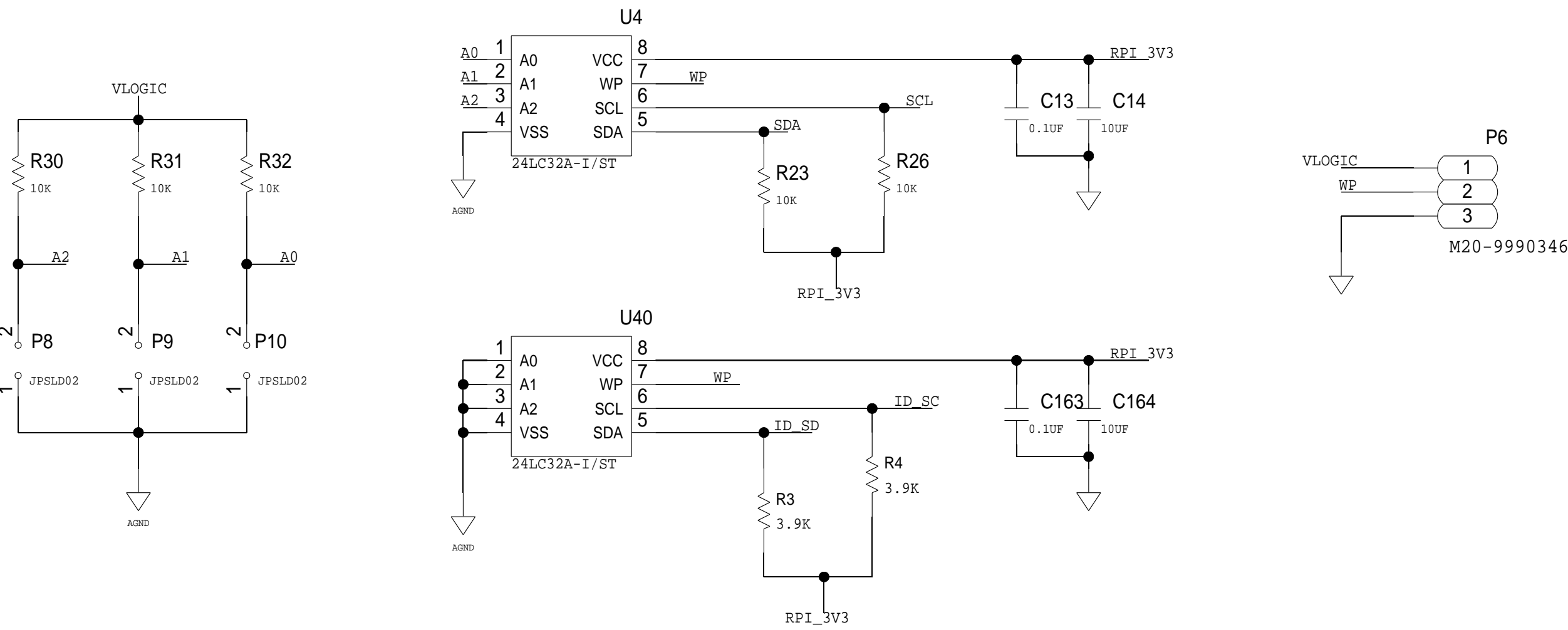
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T.CABILDO		D	<SCALE>	

LEVEL TRANSLATORS

PLUTO INTERFACE



EEPROM



	SCHEMATIC			
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SIZE D		SCALE <SCALE>		